ELECTRONICS FAULT DIAGNOSIS

Power Supplies

Audio Frequency Amplifiers

Timing Circuits

Measuring Circuits

Oscillators

Trigger Circuits

Control and Interface Circuits

Digital and Counting Circuits

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Electronics
Fault
Diagnosis

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INDEX TO SECTIONS

PREFACE

THE CIRCUITS IN THIS BOOK are typical of those found in electronic equipment, with an emphasis on industrial and communications equipment rather than on domestic equipment, and each circuit is accompanied by a fairly full explanation of the normal operation of the circuit. The circuits have also been graded within each section, so that the simplest circuits appear first. Because of this, the book can be used progressively as an aid to the teaching of servicing, in particular to those taking the C&G 272 and C&G 222 courses.

To save space, the general conditions for each problem have *not* been repeated in each question. In each set of readings or oscillograms, one set is normal, given the usual component tolerances and the use of a 20kΩ/V meter for d.c. readings. A few a.c. readings on sinewaves have been taken using a 10kΩ/V meter. In some cases, the use of such a meter may produce noticably low readings, and this must be allowed for when the readings are examined. In a few examples, the use of a conventional meter produces such low readings that the high resistance meter must be used and a FET meter with an input resistance of 100MΩ or greater has been used. The other sets of readings represent fault conditions which can be caused by the failure of a single component, though possibly more than one component can fail to give the symptoms noted.

Typical failures are those of base-to-emitter short circuits in transistors, usually along with base-to-collector open circuits, resistors high in value, capacitors short circuited, and diodes open circuit or short circuit. The oscillograms also represent failures of single components, usually failures which could not be diagnosed by meter readings alone. In some circuits, meter readings are meaningless (because of oscillation, for example), and only oscillograms are shown. Silicon transistors are assumed throughout, and the integrated circuits shown are operational amplifiers, TTL logic, or MOS circuits.

In accordance with the grading of the problems, the later examples in each section are explained in rather less detail than the earlier ones, but sufficiently to ensure that a student who has worked through the earlier problems will not find the more complex circuits impossibly difficult.

The circuits of Section VIII are not, at the time of writing, covered in the present C&G syllabus, but the rapid spread of digital methods makes their inclusion in a book of this type highly desirable. The faults in this last section

are failures of a part of an integrated circuit or of open circuit or short circuit connections, particularly when these can be caused by shorts between two adjacent printed circuit board tracks.

Answers to the problems have been given at the end of the book, together with very brief comments on the logical explanation for the answer, and in some cases suggestions on why the failure might have taken place.

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February, 1977

ACKNOWLEDGMENTS

Other Fountain books by Ian Sinclair

INTRODUCING AMATEUR ELECTRONICS
UNDERSTANDING ELECTRONIC COMPONENTS
UNDERSTANDING ELECTRONIC CIRCUITS
INTRODUCING ELECTRONIC SYSTEMS
THE OSCILLOSCOPE IN USE
AUDIO AMPLIFIERS
ELECTRONICS FOR MODELLERS

POWER SUPPLIES

I/1 half-wave rectifier supply with zener diode stabilisation

THE CIRCUIT is of a simple half-wave rectified supply which incorporates a low-voltage and low-current zener diode stabilised supply. This circuit might be used to provide power for an amplifier, with the main supply used for the output stage, and the zener stabilised portion for the preamplifier and driver stages.

As shown, the power pack is arranged for testing with a dummy load for each output, consisting of wire wound resistors. The action of the circuit is as follows. With Sw1 off, the capacitor C1 charges up to the peak voltage of the transformer secondary, which is $1.4 \times$ r.m.s. voltage, and the rectifier does not conduct when the voltage at (1) is less than the peak voltage. The zener stabilises at 12V, with the difference in voltage appearing across R1. The current taken by the zener load must not exceed the current which flows through R1 when no load is present.
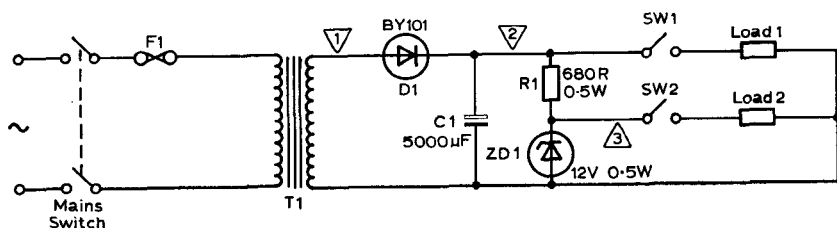
With the loads switched into circuit, the capacitor discharges through the load from the time that the voltage applied to the diode from the transformer becomes less than the peak voltage during each cycle. The capacitor will continue to discharge until the potential at point (1) is slightly positive to the potential at point (2) again, and the diode conducts. The amount by which the potential at (2) drops between peaks is not easy to calculate exactly; it depends on the time between peaks (20mS in this case), the resistance of the load, and the size (in μF) of the capacitor. The current through R1 should change very little when the zener diode load is switched into circuit, since the current into the load (2) is taken at the expense of the current flowing into the zener diode.

The table of values show voltage readings taken at each noted point in the circuit under two conditions: loaded (L) and unloaded (U).

I/1 Table of Voltage Readings

No.	1 U (a.c.)	1 L (a.c.)	2U	2L	3U	3L
1	20	19·8	9	8·8	8·9	8·7
2	20	19·5	25	20	12·2	12·1
3	0	0	0	0	0	0
4	20	20	0	0	0	0
5	20	19·5	28	20	28	18
6	20	19·4	22	18	0	0

L = on load.   U = unloaded.

I/2 full-wave bridge rectifier circuit

The circuit here is of a power supply using a full-wave bridge rectifier circuit with reservoir capacitor and choke-capacitor filter for the main supply to load (1). An additional supply at a nominal 5V is regulated by a zener diode ZD1 and supplied to load (2).

Because this is a full-wave bridge circuit, the ripple is at 100Hz (10mS

between peaks) and therefore much more easily smoothed by the filters. In addition, the difference between the no-load and the on-load voltage is less than for the half-wave circuit, since the load is supplied from the capacitor for only half as long. Off-load, the voltage output is, as before, equal to the peak voltage of the wave from the transformer. On load, the minimum possible voltage, even with no smoothing, is $0.64 \times$ peak voltage, less the drop across the resistances of the transformer secondary and choke and the drop across the rectifiers.
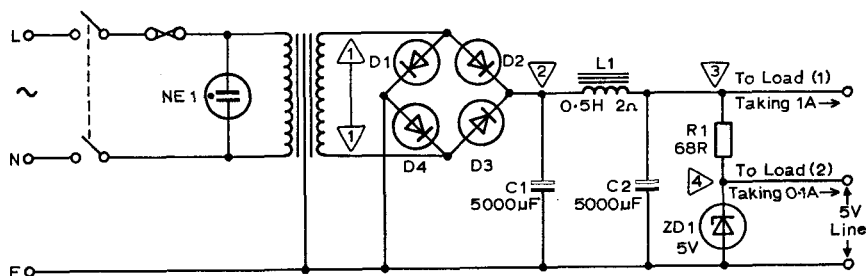
The total resistance in circuit is greater than in the previous example because of the choke and also because the current flowing from the transformer always passes through two diodes in series in any part of the cycle. Compared to the half-wave rectifier, diodes rated for a lower value of reverse voltage can be used, because the reverse voltage is always across two diodes in series.

The readings shown have been taken using a more elaborate type of dummy load which takes a constant current. Readings (a) are taken off-load, readings (b) on load.

I/2 Table of Voltage Readings

| No.	1a (a.c.)	1b (a.c.)	2a	2b	3a	3b	4a	4b
1	15	13	18·8	11·4	18·5	7·4	5·1	1·5
2	15	13	13·2	9·7	14	7·1	5·0	1·1
3	15	15	19·2	19·2	0	0	0	0
4	15	13	19·2	14·2	18·8	11·2	5·1	5·0
5	15	13	21·2	17	21·2	14	0	0
6	15	13	19·2	14·5	18·8	11·5	18·8	5·5

I/3 voltage supply with integrated regulator

The circuit shown here is of a voltage stabilised supply using an integrated stabiliser, indicated by the rectangle. The output between pins B and C of the stabiliser integrated circuit is 12V for a wide range of input voltages (which must be greater than 12V).

In the circuit shown here, the output at V_{out} has been set to 24V by using a suitably high input voltage and adding the circuit consisting of the BC477 p-n-p silicon transistor and the two bias resistors. The bias resistors act as a potential divider, so that the voltage at the base of the BC477 will be set to $V_{out} \times \dfrac{R2}{R1 + R2}$. Pin C of the stabiliser circuit will then be at a voltage about 0·6V higher than the base voltage when the transistor is returning the current of about 10mA from the regulator (acting to *sink* the current), so that $V_{out} = 12 + \dfrac{R2V_{out}}{R1 + R2} + 0·6$ volts.

The load current for test purposes is set at 250mA. and the faults shown arise either from complete failure of the stabiliser or from failure of another component.
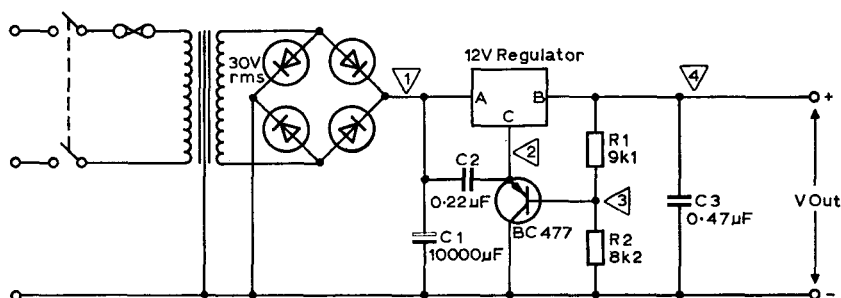
## I/3 Table of Voltage Readings

No.	1	2	3	4
1	39	0·6	0	12·6
2	39	1·0	0·4	13
3	39	10·5	10·5	22
4	39	0	18·5	39
5	39	12	11·4	24
6	26	10·6	10	23

1/4 full-wave rectified supply with thyristor and zener stabilisation

The circuit shown is an economical method of using one single power supply to give several different values of output, of which only one output is shown here. The transformer and bridge rectifier circuit provides a full-wave rectified output at a peak voltage level greater than is needed by any of the circuits which are to be supplied.

Instead of smoothing this supply, and dropping the excess voltage across a resistor or across a transistor stabiliser, a thyristor is used together with a zener diode to control each output. The thyristor conducts when its anode is positive to its cathode and also when the gate voltage has been slightly more positive than the cathode voltage. The thyristor continues to conduct, un-affected by the gate voltage, until the voltage between anode and cathode, or the current flowing, becomes too small to sustain the action of the device.
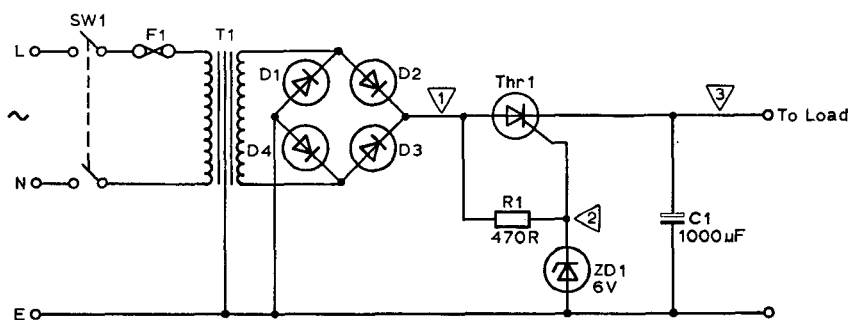
In this circuit, the gate is kept at a voltage which follows the variation of the input to the thyristor (the full-wave rectified voltage) up to the point at which the zener diode conducts. When the circuit is switched on, the thyristor will conduct on the first half cycle, charging up capacitor C1 to about the peak voltage of the supply. If no current is taken from the circuit, the voltage will remain at this peak value and the thyristor will not conduct again because its

anode is never sufficiently positive with respect to its cathode, and because the gate voltage is clipped by the zener diode at less than the cathode voltage.

With the load taking current, the voltage at point (3) will drop between the peaks of the input waveform, so that the cathode voltage may be lower than the anode voltage during peaks. The thyristor will not conduct until the voltage at the cathode is less than the voltage at the gate set by the zener diode. When this happens, the thyristor will conduct for each cycle in which the average voltage at the cathode is less than the zener voltage, and the voltage across the capacitor is topped up to just above the zener level.

Because the thyristor conducts only as needed, and is either fully on or fully off, the power dissipation in the thyristor is very low, even when there is a large difference between the rectifier output voltage and the voltage set by the zener.

Note that this circuit cannot be used in equipment which might be damaged by momentary over-voltage, since when the thyristor conducts, it will remain conducting for as long as the anode is positive to the cathode, which could mean that the capacitor is charged to the peak voltage at times.

I/4 Table of Voltage Readings

No.	1U	1L	2U	2L	3U	3L
1	10·8	10·8	0	0	0	0
2	10·8	9·8	10·8	9·8	17	15·5
3	10·8	9·8	5	5	3·9	3·5
4	10·8	10·8	5	5	0	0
5	10·8	9·8	5	5	5·3	5·2
6	17	16·5	6	6	17	15·5

L = on load.   U = unloaded

I/5 voltage tripler supply to provide e.h.t. voltages

The circuit is of a voltage-tripler power supply which might be found as
an e.h.t. supply for a photomultiplier tube. Similar circuits may be found as
supplies to cathode ray tubes or for television camera tubes of earlier design.
The principle of this and other multipler circuits is that a capacitor can block
the flow of d.c. but allow alternating current to pass fairly readily, depending
on the value of capacitance and the frequency of the a.c.
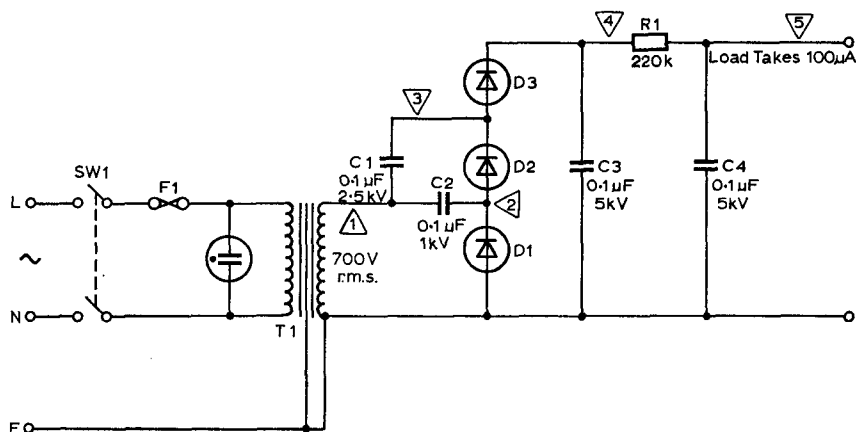
To understand the normal operation of the circuit, imagine that the a.c.
waveform at point (1) goes negative, and capacitor C2 and diode D1 conduct.
The current flowing through the diode during the negative half-cycle charges
the capacitors to the peak voltage of the sinewave, so that in the first negative
half-cycle after switching on, points (2) and (3) will charge to the peak voltage,
which is about 990V in this circuit.

  During the next positive half cycle, current will also flow through D3 into
C3, and D2 will conduct for as long as is needed to charge C3 and C1. The
next negative half cycle will 'top-up' the charge in C2, but the voltage at point

(3) will now be almost double the value of peak voltage. This happens because point (3) is already at peak volts (990V) because of the previous charging, and the connection through D2 to point (2), and is now further charged by the current flowing through C1 during the negative half-cycle.

On the next positive half cycle, this d.c. stored in C1 (now 1980V in our example) will cause D3 to conduct, charging C3. In addition, the capacitor C1 will conduct, adding another positive peak of 990V, so that C3 charges to $3 \times$ peak volts, or 2970V. With no load current flowing, C3 charges to $3 \times$ peak volts. The smoothing is carried out by the RC filter consisting of R1 (220kΩ) and C4.

The circuit is suited to small load currents (100μA in this example) at high voltage levels. The regulation is poor, meaning that the voltage will drop considerably when greater load current flows because of the high resistance of R1 and the large reactance of C1 and C2, each about 32kΩ at 50Hz. We would normally expect in this circuit to find a 'bleeder resistor' connected from output to earth to discharge C4 rapidly when the circuit is switched off. Bleeder resistors should *not* be disconnected from high voltage supplies, since their function is as a safety precaution for service engineers.

I/5   Table of Voltage Readings

| No.	1 (a.c.)	2	3	4	5
1	700	970	1940	2250	2230
2	700	0*	970	1940	1920
3	700	970	1940	2910	2890
4	700	970	970	1940	1920
5	700	970	1940	2910	1500
6	700	92	970	1940	1920

*An a.c. voltmeter read about 680V at this point.

I/6 stabilised voltage supply using discrete transistors

The circuit here is of a conventional stabilised voltage supply, using separate (discrete) transistors, to supply 15V with a load current of 0·5A. The transformer is centre-tapped, feeding a full-wave rectifier using two diodes, and the output is smoothed by C1. The voltage output here is, as usual in stabilised circuits, considerably greater than the stabilised voltage output, and will vary considerably with changes in the mains voltage and in the current taken by the load.

Tr3 is the series stabiliser stage, with the load in its emitter circuit, and the 6V (nominal) zener diode, ZD1, acts as a reference voltage, fed with a current of about 15mA through R4. A fraction of the output voltage is selected by the chain R6,VR1,R7, whose values are chosen so that the voltage at point (5) can be made greater than the zener voltage.

In normal operation, the voltage level at point (5) exceeds the zener voltage by enough to make Tr4 conduct, and the voltage level at point (4) is used, by way of the current amplifier Tr2, to control the base voltage of Tr3. A rise in the voltage at point (5) causes greater current in Tr4, a drop in voltage at point (4), and so less bias to Tr3, so acting to lower the voltage by reducing the current through Tr3. A drop in voltage at point (5) will have the opposite
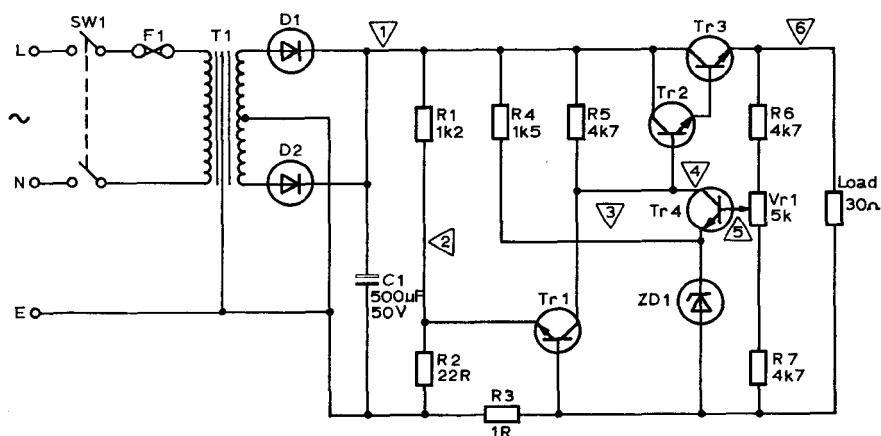
effect, so that stabilisation is obtained as long as the transistors are biased within their normal working range.

Tr1 is normally biased off. The voltage level at its emitter due to the potential divider R1,R2, is opposed by the voltage drop across R3, a small value resistor, when the nominal maximum current of 0·5A flows. Excessive current flowing in R3 causes the base of Tr1 to switch on, since the emitter will be sufficiently negative with respect to the base. Note that the earth connection is made on the load side of R3, so that the polarity of the voltage on the transformer side of R3 measured with respect to earth is *negative*. With Tr1 switched on, the voltage at point (4) is reduced, so that Tr3 is biased back. This lowers the output current, keeping the output voltage low and protecting even against a short circuit across the output.

In the table of values, one set of readings is normal, but in the remaining readings a fault exists which makes the output voltage abnormal, and adjusting the voltage set potentiometer VR1 has no effect.

I/6 Table of Voltage Readings

No.	1	2	3	4	5	6
1	29	0·6	5·8	6·0	2·2	5·0
2	20·6	—0·7	5·8	0·6	0	0
3	23·5	0·01	5·8	16·7	6·5	15
4	29	—0·6	5·8	0·6	0	0
5	21·7	—0·3	21·6	21·3	8·2	19·5

# I/7 d.c. to d.c. converter

The circuit is of a d.c. to d.c. converter used for running nuclear counter equipment from a 12V car battery. The two power transistors Tr1 and Tr2 are arranged in an oscillator circuit, with the collectors fed through the centre-tapped primary winding of the transformer T1. The oscillator circuit is self-starting, because any change in the collector current drawn by one of the

transistors will cause an opposite change in the voltage at the other collector because of the transformer action, and this voltage will also be coupled (by C1 and C2) back to the bases of the transistors.

The frequency of operation is high, about 1kHz, which is high enough to ensure that a very small transformer can be used, but not so high that the transistor switching time is an appreciable fraction of the cycle time. Since the output is a squarewave, and the switching times are short, the dissipation in the transistors is very small compared to the amount of power switched. At the output, the 1kHz square wave is rectified in a full-wave bridge, using a comparatively small value of reservoir capacitor because of the high frequency.

When faults develop in a circuit of this type, care must be taken to avoid over-dissipation in the power transistors. If oscillation stops for any reason, one or both transistors will pass large currents, limited only by the resistance of the transformer windings.
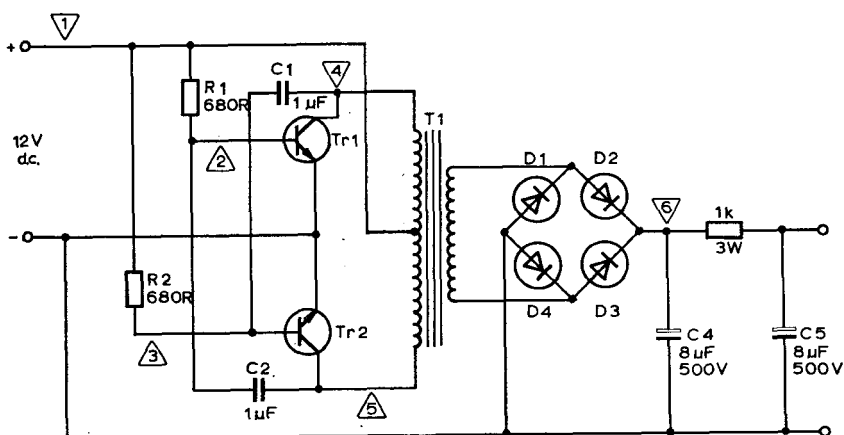
I/7   Table of Voltage Readings

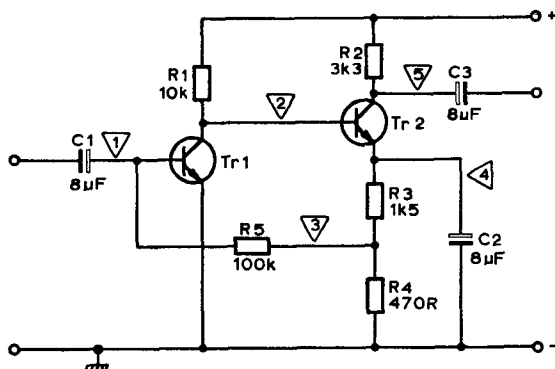| No.	1	2	3	4	5	6
1	12	−5	−5	6·5	6·5	191
2	12	−5	−5	6·5	6·5	300
3	11	1·1	1·1	0	2·3	0
4	11	1·1	0	2·2	11	0
5	12	−0·6	−2·4	2·8	8·2	85
6	12	−5	−5	6·5	6·5	96

AUDIO FREQUENCY AMPLIFIERS

II/1 two-stage a.f. amplifier with direct coupled transistors

THE CIRCUIT shown is of a common type of two-stage audio amplifier in which the transistors are direct-coupled and the bias is set by the feedback from the junction of R3 and R4, through R5, to the base of Tr1. This feedback loop is effective only at frequencies lower than that set by the value of the time constant in the emitter circuit of Tr2, and so has no effect on the gain at audio frequencies, though it stabilises the bias, and also reduces the gain at very low frequencies.

The normal gain of the circuit is high; depending on the values of load resistances at input and output, the voltage gain could be about 700 times (57dB) if another similar stage of amplification is being driven. Most of the gain is due to Tr1, which uses a fairly high value of load resistor and a comparatively low collector current.

Because of the feedback bias circuit, changes in any of the components round the feedback loop will affect all of the voltage readings, and some care is needed if the appropriate fault is to be identified. The fault conditions which are tabulated will all cause either zero output signal or severe distortion of wave-shape when a normal input signal is applied. The voltage readings in the table have been taken with no input signal applied.

II/1 Table of Voltage Readings

No.	1	2†	3	4	5
1	*	2·3	0·4	2·3	15
2	*	3·8	0·8	3·6	9
3	*	5·3	1·3	5·5	5·8
4	*	10	0·5	10·6	10·8
5	0	5·7	1·3	5·6	5·7
In the following case, the gain on the amplifier is very low					
6	*	3·8	0·8	3·6	9

*indicates a very small reading.
†in column (2), readings about 10% higher were obtained using a FET-meter.

II/2 low power amplifier with Class A output

The circuit is of a small amplifier of low output used in a baby-alarm circuit, supplied from a mains power pack. The output stage is a Class A type using a 2N697 transistor operated very close to its maximum dissipation, so that a heat-sink is used for this transistor.

Current drive is supplied to the base of the output transistor by an emitter follower, again a 2N697, which is direct coupled to the collector of the voltage amplifier stage, Tr1. This first stage, using a BC108, is run with a low collector current to minimise noise, and with a large value load resistor to ensure a

reasonable figure of voltage gain. With no load, the voltage gain of Tr1 would be about 300 times (49·5dB), and the gain is not too severely reduced by the connection to the base of Tr2, because of the fairly high input resistance of Tr2 in the emitter-follower connection.

In any Class A circuit, the bias stabilisation of the output stage is important, particularly when the output transistor is operated fairly close to its maximum dissipation value. In this circuit, bias stabilisation is carried out using a bias feedback loop from the emitter of Tr3 to the base of Tr1, so that all three transistors are included in the feedback loop. As with any feedback loop, any change in the components within the loop will cause changes in all the voltages measured. A small amount of signal feedback is also introduced by leaving R2 undecoupled.

We can assume that the amplifier faults have resulted in zero or distorted output signal, and that the voltage tests are carrried out with no a.c. signal applied.
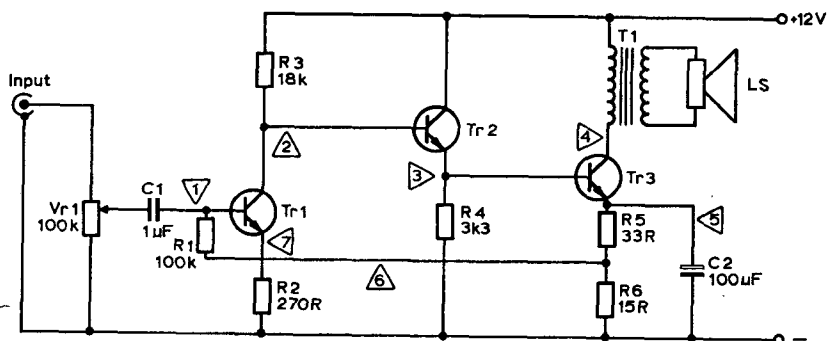
II/2   Table of Voltage Readings

No.	1	2†	3	4	5	6	7
1	*	3·8	4·0	9·7	3·3	1·0	*
2	*	3·8	4·0	12	3·3	1·0	*
3	0	*	0	12	0	0	0
4	0	6·4	7·5	7	6·9	0	0
5	0	0·5	0·5	12	*	*	0
6	0	6·4	7·6	7	6·9	2·1	0

*indicates a very small reading.
†indicates that readings about 20% higher could be obtained using a FET volt-meter.

II/3 medium-power Class B output stage using 'totem-pole' circuit

Shown here is a medium-power Class B output stage for an audio amplifier, actually one channel of a stereo amplifier. The output pair of transistors form a complementary single ended push-pull stage, sometimes called the 'totem-pole' circuit.

Tr3 and Tr4 are biased by the voltage across the collector-emitter of Tr2, so that the quiescent (with no signal in) current passed through the output transistors is fairly small, about 10–15mA. The voltage level at the junction of R7,R8 is stabilised by the feedback through VR1 and R1 to the base of Tr1, with direct coupling over the remainder of the circuit. In this case, a.c. as well as d.c. is fed back, though several amplifier stages of this type use an extra p-n-p transistor in the feedback loop and aim for an a.c. gain of about 20 times (26dB) and d.c. gain sufficient to stabilise the operating conditions of the output pair and the driver.

The use of Tr2 to develop the bias voltage for the output pair assists greatly in keeping bias stable when temperature fluctuates. The effect of
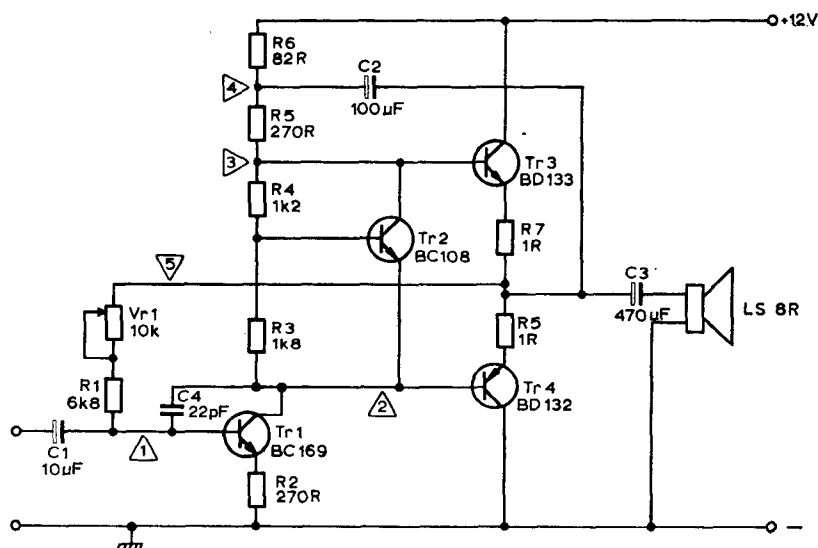
rising temperature on a silicon transistor is mainly to reduce the voltage between base and emitter for a given collector current. In this circuit, a rise in temperature will increase the bias current in Tr2, bringing this transistor nearer saturation and making the voltage across it less, so that the bias on the output pair decreases.

The connection of capacitor C2 has no effect on the steady bias readings, but forms a 'bootstrap connection' for audio frequencies. With signal input, capacitor C2 drives the junction of R5 and R6 so that the current in R5 can be kept flowing even when the voltage at point (3) is nearly 12V, so avoiding the severe distortion which would occur if the same level of drive were used without this connection.

Note that the quiescent current is not adjustable in this circuit; it is set by the bias on Tr2. The preset VR1 is used to trim the voltage level at point (5).

In the fault conditions shown, normal input to the stage has resulted in zero or distorted output. The amplifier is then tested with normal d.c. applied but with no a.c. signal in.

II/3   Table of Voltage Readings

No.	1	2	3	4	5
1	0·9	6·2	6·4	10·7	5·9
2	0·4	0·6	1·6	11·7	1·1
3	*	11·9	11·9	11·9	11·4
4	*	1	2	4	1·5
5	0·9	5·4	6·6	10·7	6·0

6 This fault makes it impossible to obtain readings, since the supply fuse blows repeatedly. C3 is tested and found to be normal, and the 8 ohm speaker is also found to be perfect.

*indicates a very small reading.

II/4 audio preamplifier with disc playback equalisation circuits

The circuit shown is of an audio preamplifier with equalising circuits for disc playback. Most of the gain is provided by the use of a type 741 integrated circuit, whose gain and operating conditions are stabilised by feedback. Because this circuit is intended for low amplitude inputs (from a magnetic pickup cartridge) the noise level at the input is important, and so the input is not taken to the 741 directly because of the comparatively high noise generated by this IC. Instead, a balanced circuit using BC108's is used, with very low values of collector currents so as to reduce the noise generated in the transistors.
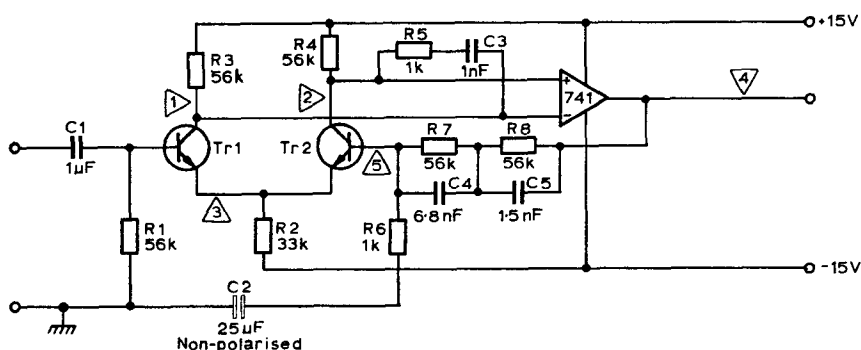
Because noise is random and will not be identical in the two transistors, the balanced feed to the 741 does not cancel any high frequency noise, but does greatly reduce any hum pickup from the power supply line or into the input leads. In addition, the balanced input stage makes it possible to isolate the feedback loop from the input, so that changes in the impedance of the input when different cartridges are used does not alter the amplifier operating conditions.

The action of the 741 is such that, given approximately equal voltages at the

two inputs, close to zero, the output will be at zero volts when a balanced (equal positive and negative lines) power supply is used. Raising both input levels above zero volts will cause some change at the output, but this can be compensated for, and so the output level reduced to zero, by a very small change of either steady input voltage relative to the other; only a few millivolts of this 'offset' correction will be needed.

The d.c. feedback loop from the output of the IC to the base of Tr2 ensures the correct operating conditions for the IC provided that there is no fault in the components round the feedback loop, and that the correct voltage levels can be maintained. The components C3,R5 play no part in the bias, but serve to make the resistance between the balanced inputs low at the higher audio frequencies, reducing the risk of high-frequency oscillation. The very high gain of an IC operational amplifier means that precautions must always be taken against oscillation, since the output pins are never very far distant from the input pins.

II/4   Table of Voltage Readings

In this particular circuit, all the readings have been measured using a FET voltmeter.

No.	1	2	3	4	5
1	15	15	0	−12	−12
2	13·8	13·8	0·5	0	0
3	2	2	−0·5	0	0
4	0·1	0·1	−0·5	0	0
5	15	11·7	11·5	12	12
6	−0·4	15	−0·5	−12	−12

II/5 high input impedance circuit
using two direct-coupled transistors

The circuit used in this example is a common type of high input impedance circuit found when for some reason MOSFET circuits are not considered suitable. Considering the circuit first of all from the point of view of bias alone, Tr1 is connected as an emitter-follower with a very small collector current, biased by the connection of its base through R3 to the junction of R1 and R2. The small currents in Tr2 are used to drive the current amplifier, the p-n-p transistor Tr2, directly coupled to Tr1 and with 100% feedback through the connection of Tr2 collector to Tr1 emitter. Tr2 then supplies the current which provides the voltage across R4.
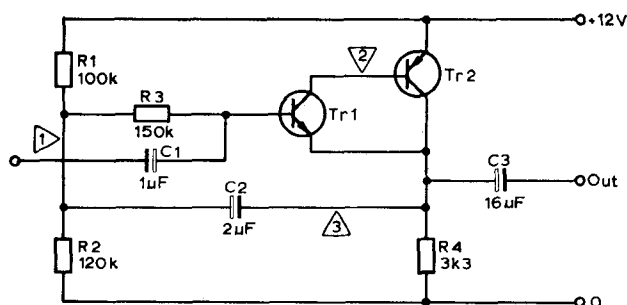
Without the use of C2, the input resistance of the circuit would be reasonably high but limited by the values of the bias resistors. The use of C2 means that signals at the output appear also at the junction of R1 and R2 with almost the same amplitude as the input signal through C1. This in turn makes the amount of signal current flowing through R3 very small, so that the circuit behaves as if R3 had a very high resistance to signal currents. Because of this 'bootstrap' connection, a form of positive feedback, the input resistance to signals can be several megohms.

In the fault conditions shown, readings have had to be taken using a FET (or valve) voltmeter because of the high resistances used in the circuit. In all the fault conditions, a normal input has resulted in a low amplitude or distorted output. The readings shown have been taken with no signal input.

II/5   Table of Voltage Readings

All the readings have been taken using a FET voltmeter.

No.	1	2	3
1	6·5	11·5	6·0
2	*	12	*
3	6·5	12	*
4	4·8	12	*
5	11·8	11·5	11·0
6	0	12	0
7 In this case, normal voltage readings are obtained, but the input resistance is low.			

*indicates a very small reading.

II/6 interface circuit amplifying pulses from a light beam detector

Logic circuits are very often driven by audio-frequency pulses obtained from other circuits such as tape readers, punch card readers, or along telephone lines, and pulse amplifiers may have to be used between the source and the logic circuit input. In the language of computer engineers, an interface circuit is needed. The circuit shown here is an interface circuit which amplifies pulses from a light-beam detector. The pulses are of reasonably large amplitude but come from a high impedance source and cannot drive the TTL logic gates, which need driving currents of about 1·6mA at their inputs.

The TTL gate, IC1, has one input connected to the +5V line, and will give an output which is low (less than 0·5V) when the other input is high (more than 2·5V). In this state, the inputs to the gates pass a very low current, a few μA. With no pulse input at Tr1, the connection of the base of Tr3 to the

negative rail through R2 ensures that Tr3 conducts, and the input of gate IC1 is connected to the negative rail through Tr3. In this condition, the gate input passes a current of about 1·6mA through Tr3; we say that Tr3 is being used to sink a current of 1·6mA.

When a positive pulse appears at the input to Tr1, the connection of diode D1 from the emitter of Tr1 to the base of Tr3 will cause Tr3 to cut off, so that the voltage at point (4) can rise sharply. It is important that the voltage changes at the input to a logic gate should be very rapid, since the gate can oscillate if the rise and fall times are too long (as long as a microsecond, for example).

In most practical cases, an additional safeguard would be provided by making IC1 a 'Schmitt' type gate (see later) which has a trigger action and which will switch over rapidly even if the input waveform is slow to rise or fall.

In the fault conditions shown, the action of the gate has been faulty. Readings are taken with point (1) returned to the +5V line so as to check the operating voltages on the transistors.
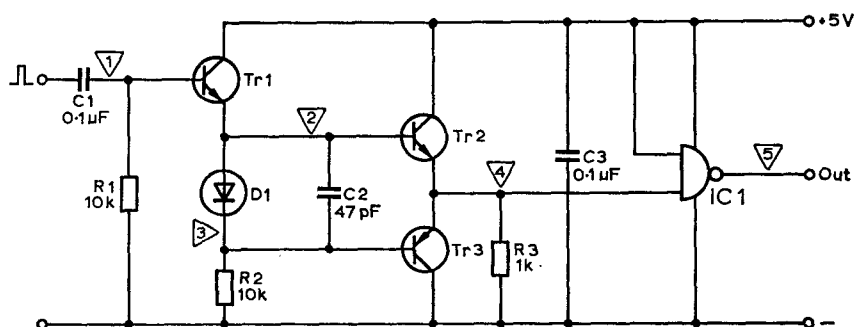
II/6   Table of Voltage Readings

This circuit is tested with point (1) returned to the positive supply.

No.	1	2	3	4	5
1	5	4·4	4·4	3·8	0·2
2	5	4·4	3·8	3·8	0·2
3	5	4·3	3·7	4·3	0·2
4	5	4·4	4·4	3·8	0·2
5	5	5	4·4	4·4	0·2
6	5	4·4	3·8	3·8	0·2

II/7 receiver for light-beam system

The use of an amplitude-modulated light beam can be convenient for short-distance communications, and the circuit shown here is a receiver for such a light-beam system. Modulated light hitting the phototransistor causes a signal current to flow into the amplifier through the coupling capacitor C1. The operational amplifier is connected with resistors R3 and R4 and capacitor C2 to provide d.c. feedback, so stabilising the bias voltage at the −input at around zero volts. Resistor R5 then sets the gain of the amplifier. The amplified signal at the output of the operational amplifier is coupled through C3 to the base of Tr1, a power amplifier operating in Class A and transformer coupled to the loudspeaker.

In the fault conditions shown, the receiver has given zero or distorted output when the input signal has been normal. For testing, the input phototransistor has been illuminated with a steady unmodulated light beam, and the readings at point (1) have been taken using a FET voltmeter.
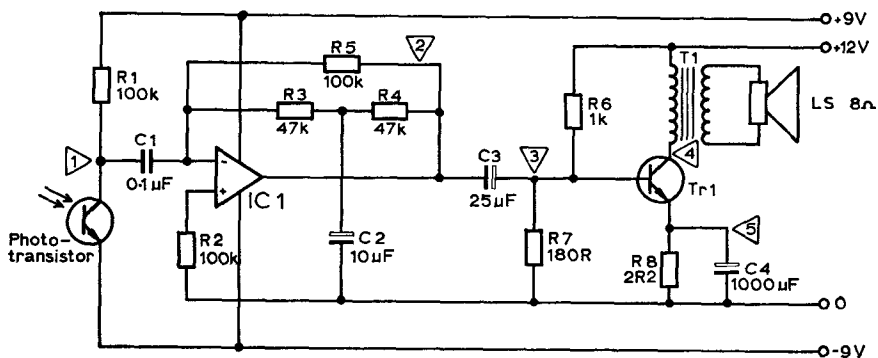
II/7 Table of Voltage Readings

No.	1	2	3	4	5
1	−9	0	1·7	11·2	0·1
2	1	0	0·2	12	0·1
3	1	0	1·8	12	1·3
4	1	0	*	12	*
5	1	0	1·7	10·2	0·1
6	1	0	0·8	10	0
7	9	0	1·7	10·2	0·1

*indicates a very small reading.

II/8 logic circuits at audio frequencies driving solenoids

Interfacing may also be a problem at the output of a logic circuit. In this example, logic circuits operating at audio frequencies are used as part of a process controller, with the outputs used to drive solenoids which control mechanical operations. One solenoid is energised when the inputs to the gate at point (1) are high, the other is energised when the inputs to the gate are low. The gate action is that of an inverter, with the output voltage low when the inputs are high, and with the output voltage high when the inputs are low.
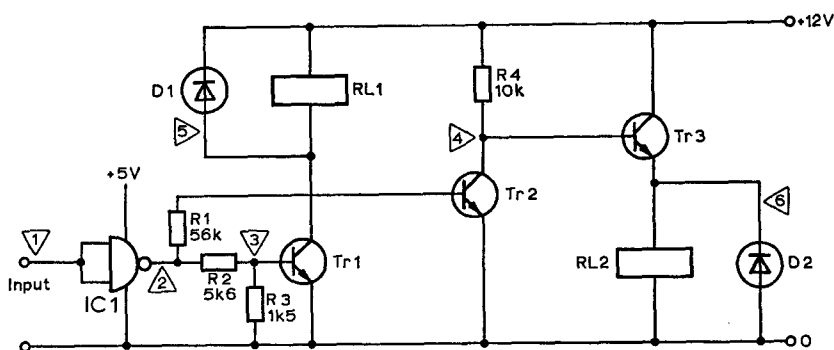
A high output voltage drives current into the base of Tr1, so that collector current flows, energising solenoid 1, which passes about 35mA. A low output turns off Tr2, allowing its collector voltage to rise and switch on Tr3. The solenoid, again taking about 35mA, is connected in the emitter circuit of Tr3. In each case, diodes are connected across the solenoid windings to avoid damage to the transistors when current is switched off and a reverse voltage is generated by the change of current in the high-inductance solenoid winding.

In the circuit shown, the action of one or both solenoids has been faulty, and the unit has been removed for testing. Testing is carried out by taking measurements of voltages with the input (1) taken to the +5V rail (ON) and again with the input (1) taken to the ground line (OFF).

II/8   Table of Voltage Readings

This circuit is tested both with the IC gate ON and OFF.

No.	1	2	3	4	5	6
1	ON	0	0	11·5	12	11·4
	OFF	0	0	11·5	12	11·3
2	ON	0·1	*	11·5	12	11.5
	OFF	4·5	0·4	*	12	0
3	ON	0·1	*	11·5	12	11·3
	OFF	4·5	0·7	*	0·3	0
4	ON	0·1	*	1·8†	12	2·3
	OFF	4·5	0·7	*	0·3	0
5	ON	0·1	*	11·5	12	11·3
	OFF	4·5	0·7	11·5	0·3	11·3
6	ON	0·1	*	11·5	12	11·3
	OFF	4·5	0·7	*	12	0

*indicates a very small reading.
†indicates that a higher reading could be obtained using a FET voltmeter.

TIMING CIRCUITS

III/1 analogue-to-digital converter

AN ANALOGUE-to-digital converter is a type of circuit whose input is a steady or slowly-varying voltage, and whose output is a set of pulses whose frequency depends on the value of voltage at the input. In this circuit, the voltage level at the input is used to set the time interval between pulses which are generated by a unijunction.

The action of the unijunction, Tr2, is that a small current flows between the two base contacts while the voltage applied to the junction is low. The resistance between the base contacts is about $7k\Omega$ in this instance. Whenever the junction voltage reaches about 0·6 times the voltage between the bases (in this case, $0·6 \times 12 = 7·2V$), then the junction conducts with a low resistance to the base terminal at the lower voltage, so that a large amount of current can flow.

In this circuit, the voltage at the input controls the current in resistor R1. This current, together with current through R2 controlled by the bias voltage, is the base current for the p-n-p transistor Tr1. The collector current flowing
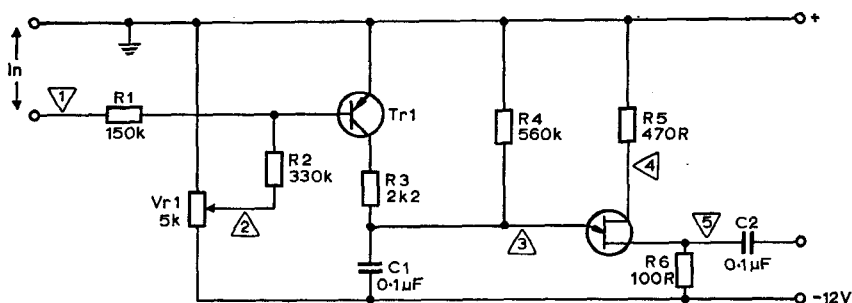
through Tr1, under the control of its base current, charges C1 through the limiting resistor R3. When the voltage across C1 reaches the firing voltage of the unijunction, the unijunction conducts, so connecting C1 to the 100Ω output resistor, so that a short pulse of voltage is obtained as C1 discharges. When C1 has discharged the unijunction shuts off again, and the process is repeated.

If the charging current is very small, the time between pulses is fairly long, several tens of milliseconds. If, due to a larger value of input voltage, the charging current is greater, the time between pulses is considerably less. Because the charging current is controlled by Tr1, the frequency of the output pulses is proportional to the input voltage between the input terminals.

Since the circuit voltages all vary during normal operation, there are no useful 'normal' voltage readings, and the readings shown represent fault conditions in which oscillation has stopped or become very slow. The oscillograms shown include one normal set of traces and various fault conditions.
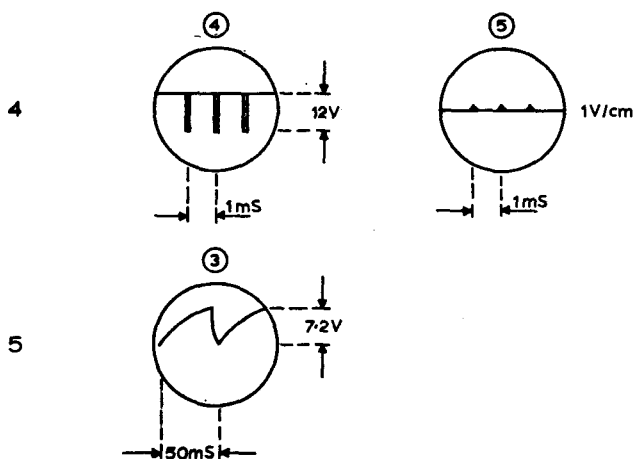
III/1 Table of Voltage Readings

There are no useful 'normal' meter readings. In questions 1–3, the converter has stopped giving output pulses, or the oscillation rate is abnormally slow.

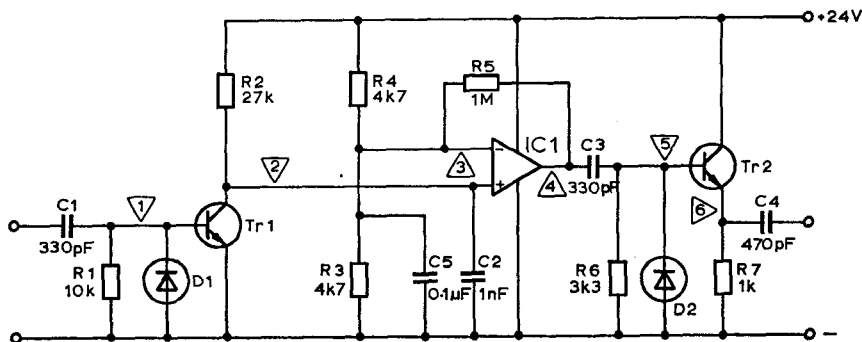| No.	1	2	3	4	5
1	5	8	0	12	0
2	5	8	12	12	0
3	5	8	slow oscillation only		

III/2 time delay circuit using a 741 operational amplifier

One important application of timing circuits is to generate time delays, so that an output pulse is obtained at some fixed or, possibly, variable time later than an input pulse. The circuit shown here uses a type 741 integrated operational amplifier as a part of a time delay circuit used to delay an oscilloscope trigger pulse so that the leading edge of a long pulse can be examined.

The positive-going pulse at the input is differentiated, and the leading edge used to switch on Tr1 momentarily. The momentary conduction of Tr1 discharges C2, making the voltage at the + input of the IC almost zero. This in turn makes the output voltage of the IC almost zero. Capacitor C2 now charges through R2 towards the 25V supply line. When the voltage at the + input reaches a level about equal to the voltage set by R4,R3 at the − input, then the operational amplifier switches over from zero output to high-voltage output (nearly supply voltage). The switch-over is very rapid, and the operational amplifier will stay in this state until the next pulse arrives.

The rising edge of the output pulse is differentiated by C3,R6 and applied to the base of Tr2, giving an output pulse across R7. The falling edge which occurs when Tr1 conducts is removed by diode D2. Because of the charging time set by R2,C2 (time constant 27μS in this example), the pulse at the output is delayed by several microseconds compared to the pulse at the input.

The tests in this example have been carried out by using a voltmeter and an oscilloscope. The voltmeter tests are carried out by taking readings firstly with no input (OFF), and then with test point (1) connected to the +25V line through a 47kΩ resistor (ON). The oscilloscope tests are carried out with a 1μS pulse input from a pulse generator. Assume that the oscilloscope has been triggered just before the pulse enters the delay, by using the 'pre-pulse' trigger output which is provided on high-quality pulse generators.

III/2   Table of Voltage Readings

Two sets of readings are taken, the OFF readings with no input, and the ON readings, with a resistor connected between point (1) and a positive voltage line.

No.	1	2	3	4	5	6
1 OFF	0	24	12·5	23	0	0
1 ON	*	24	12·5	23	0	0
2 OFF	0	24	12·5	23	0	0
2 ON	0·7	0·1	12·5	1·5	0	0
3 OFF	0	24	12·5	23	0	0
3 ON	0·7	0·1	12·5	23	0	0

*indicates a very small reading.
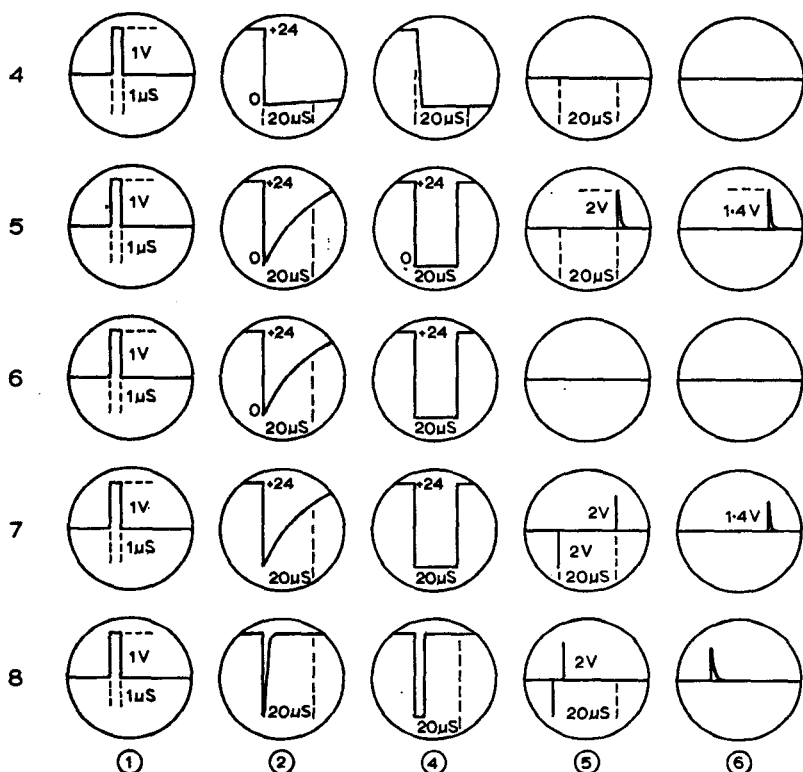
III/3 timing circuit using a 555 IC

Timing circuits are used so extensively that an integrated circuit has been designed as a timing circuit capable of a very wide range of applications. In the type 555 timer circuit, pin 2 is the trigger connection, and timing starts when the voltage at pin 2 is taken momentarily low; at which time the voltage on pin 7 is about one third of the supply voltage.

The timing part of the cycle is carried out by charging a capacitor C3 through resistors R3, R4 (in this example). When the voltage across C3 reaches a level equal to two-thirds of the supply voltage, an internal switch changes over, connecting pin 6 to pin 1 (which is grounded) and so discharging the capacitor very rapidly, and preparing it for the next cycle. At the same time, the internal switch is connected to pin 3 so that the voltage at pin 3 is high while the voltage at pin 7 is less than 2/3 of supply voltage, and low when the switch operation discharges C3.

The action of the switch circuit inside the 555 is such that the discharge of the capacitor continues until the voltage across it is one third of the supply voltage, since these are the voltage limits set within the timer and triggered by pin 7. Other voltage limits can be set externally if needed.

In this circuit, a 555 timer has been used in a circuit designed to generate a pulse a short time after the whole circuit has been switched on. This might, for example, be used to reset a counter each time the supply was switched on. When the switch Sw1 is switched on, current flows to the timer circuit through D1 (used with C1 to protect against negative-going pulses) and capacitor C2 starts to charge through R1.

The voltage to which C2 can charge is limited by the connection of R2 to earth line. C2 is connected to the trigger pin, 2, and since pin 2 must be at a low voltage for timing to start, the timing starts whenever Sw1 is switched on. C2 then charges quickly, so that pin 2 voltage reaches a level greater than its triggering value long before the end of the timing cycle. This is essential, because the timing cycle cannot be completed while the voltage on pin 2 is low.

The timing capacitor C3 is also charging up during this time, and when the voltage across it reaches 8V (2/3 × 12V in this example) the circuit switches
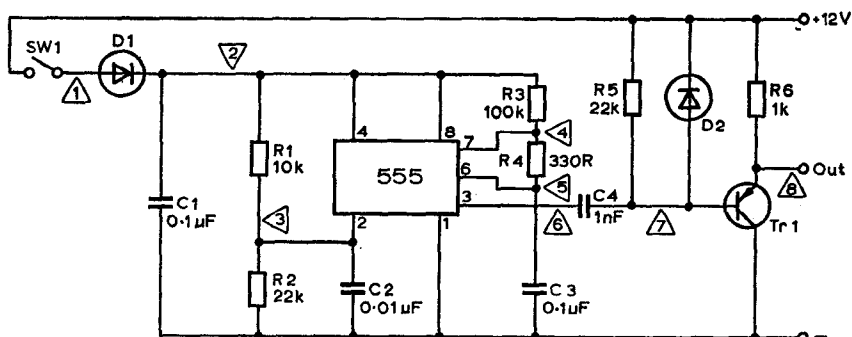
over, discharging C3 to ⅓ of line voltage (4V in this case) and making the output voltage on pin 3 go low. The negative-going edge caused by this change is differentiated by C4,R5, and drives Tr1 momentarily into conduction, giving a negative-going pulse at the emitter of Tr1. This pulse is delayed several milliseconds from the closing time of Sw1. No further pulses can be generated unless Sw1 is opened, allowing C2 to discharge through R2, and then closed again, so that the cycle repeats.

The meter readings in this instance have been taken a second or so after Sw1 was switched on, and one set is normal. The oscillograms have been taken using a storage oscilloscope (which retains a trace for several minutes).

| No.	1	2	3	4	5	6	7	8
1	12	12	8·3	*	*	*	12	12
2	12	12	8·3	*	*	*	12	12
	(in this case, the time delay is very long)							
3	12	0	0	0	0	0	12	12
4	12	12	2	9·6	9·6	12	12	12

*indicates a very low reading
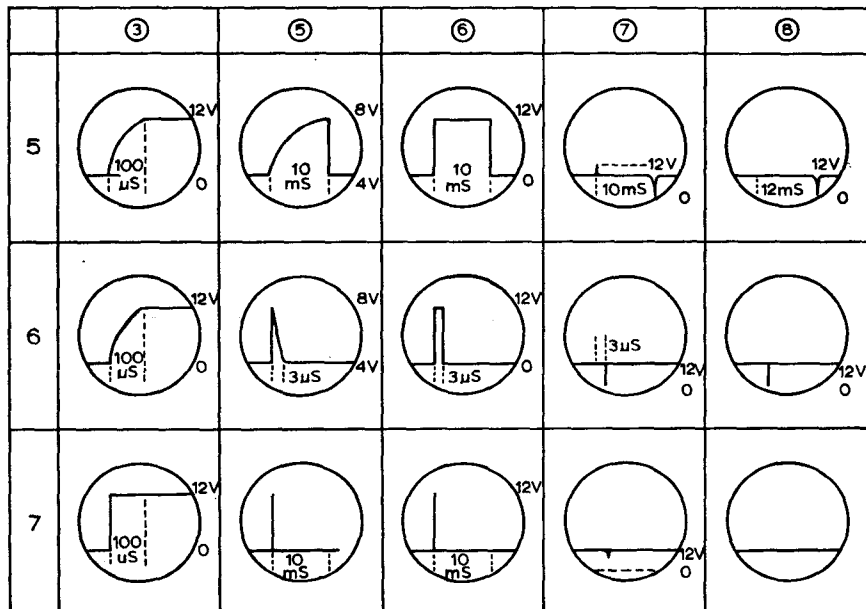
III/4 timing circuit using discrete transistors

The diagram shows a timing circuit using two general purpose or switching transistors. With no pulse input, Tr1 is held in conduction by the return of its base through D2 and R1 to the positive line. This in turn keeps Tr2 switched off, since its base is fed through R5 and R6 from the collector of Tr1. C3 acts as a 'speed-up' capacitor, so that rapid changes of voltage at the collector of Tr1 are passed directly to the base of Tr2 with no attenuation by the resistors.

When a negative-going input pulse, which must have a fast leading edge, is applied to the input, Tr1 is switched off, and the collector voltage of Tr1 rises rapidly. The rise in voltage is communicated to the base of Tr2, switching Tr2 on, so that the collector voltage of Tr2 falls sharply. This releases the base of Tr1 by making the voltage at the anode of the diode D2 low, so that Tr1 is held off, but without applying any negative voltage. Additional trigger pulses can now have no effect, because D1 is reverse biased by the return of its emitter to the collector of Tr1 through R3.

C2 now charges up through R1 for the timing action of the cycle. When the voltage at the base of Tr1 reaches the switch-on level, Tr1 conducts, and its collector voltage level drops. This in turn switches off Tr2, whose collector voltage rises, reinforcing the switching of Tr1 because of the link through C2 and D2.

A common fault of timing circuits is 'jitter', small changes in the switch-back time which cause the delayed pulse to appear to move slightly from side to side when shown on an oscilloscope display. This circuit attacks the problem of jitter by using the diodes D2 and D3. D2 ensures that the charging circuit for C2 is not loaded by the base of Tr1 until D2 conducts; and D3 isolates the timing capacitor C2 from any negative pulses present in the supply line, particularly at the critical time near the end of the timing period. The output pulse is differentiated by C4,R7, and the trailing edge is selected by D4 so that the output is a narrow pulse delayed by an amount of time set by the values of R1 and C2.
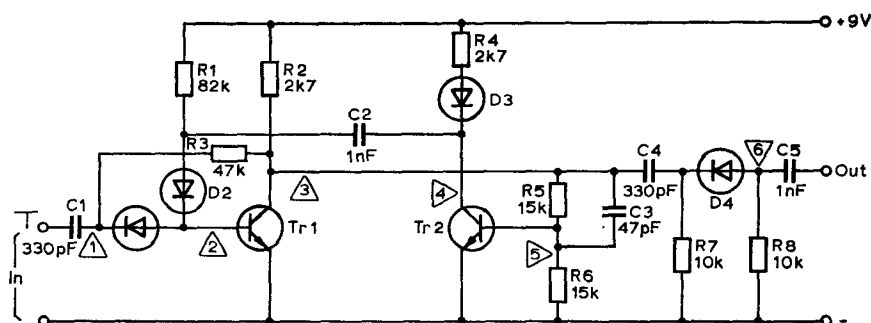
In the circuit shown, the voltage readings are taken with no pulse input, and the oscilloscope readings are taken with a 1μS, 1V amplitude negative-going pulse input. One set of each is normal, the others represent fault conditions.

III/4 Table of Voltage Readings

No.	1	2	3	4	5
1	*	0·7	0·4	0	0·2
2	*	0·7	0·4	9	0·2
3	6·6	*	8·2	0·4	0·7
4	*	0·7	0·4	9	*
5	0·7	0·7	0·4	9	0·2

*indicates a very low reading.

Input in each case
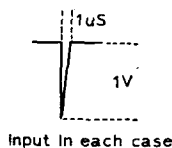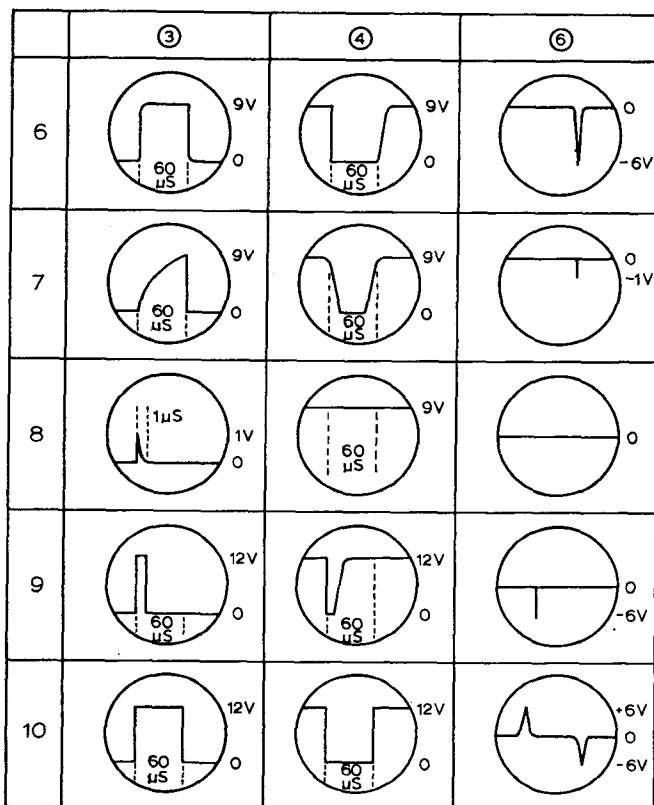
III/5 fixed-frequency timebase

Linear sweep generators are used extensively in timebases and in other timing circuits, and consist of a squarewave generator coupled to an integrator. The simple circuit shown here is typical of fixed-frequency timebases; it uses a squarewave from a fixed frequency oscillator to give a timebase output of fixed frequency and amplitude.

In the circuit shown, Tr1 is a switching transistor which is cut off or saturated according to the output of the multivibrator which drives the base of Tr1. Tr2 is a linearising stage for the sawtooth waveform. Imagine that Tr1 has just been shut off by the signal from the multivibrator going negative. The voltage across C1 will be very low, since Tr1 has been saturated. C1 now starts to charge through R1 and VR1 towards 15V. As the voltage across C1 rises, the base voltage of Tr2 will rise until current flows in Tr2, when its emitter voltage will also start to rise.

The connection of the zener diode to the junction of R3 and R1 ensures that the voltage at this point will rise by the same amount for as long as the voltage across the zener diode can be maintained, and will be 9V greater than the voltage at the emitter of Tr2 for a range of voltages. The use of the zener diode in this way ensures that the voltage across R1 and VR1 is constant (at about 9V less the base-emitter drop of Tr2) during part of the charging period of C1, so that the current into C1 is constant during this time. This ensures a linear rise of voltage.

Before the voltage level at the junction of R3 and R1 can reach 15V, Tr1 is switched on again by the multivibrator, so that C1 is rapidly discharged, and the voltage levels in the rest of the circuit are returned to their starting levels. Tr3 is a buffer stage which gives an output only during the linear part of the cycle when Tr2 is conducting.

The meter readings shown are taken with the circuit disconnected from the multivibrator, so that two sets of readings can be taken. One set is taken with the base of Tr1 earthed; the other with the base of Tr1 returned to the +15V line through a 15kΩ resistor. The oscillograms are taken with a pulse input as shown, with a 5μS on time and 50μS off time.
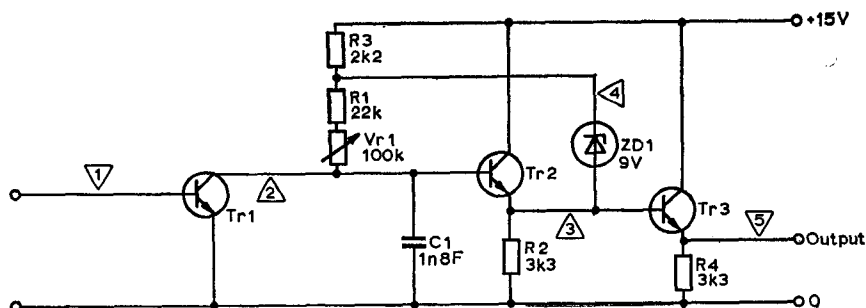
These are static tests taken with the base of Tr1 returned either to earth (0) or through a resistor to a positive voltage (0·7).

No.	1	2	3	4	5
1	0 0·7	1·5 0·2	14·4 3·6	15 12·6	13·8 3·0
2	0 0·7	3·6 0·2	3·6 0·2	12·6 9·2	3·0 0
3	0 0·7	15 0·2	14·4 0	15 15	13·8 0
4	0 0·7	0·2 0·2	3·6 3·6	12·6 12·6	3·0 3·0
5	0 0·7	15 0·2	14·4 1·8	12 13·8	13·8* 1·2
6	0 0·7	15 0·2	14·3 1·8	15 10·8	14·3 1·8

The figures of point (2) have been obtained using a FET voltmeter.

*no speed control.

	①	④	⑤
7	5µS / 50µS, 1V, 0	50µS, 15V, 11·6V	50µS, 14V
8	5µS / 50µS, 1V, 0	50µS, 13·6V, 11·6V	50µS, 2V
9	5µS / 50µS, 1V, 0	50µS, 0·3V	50µS, 0·3V
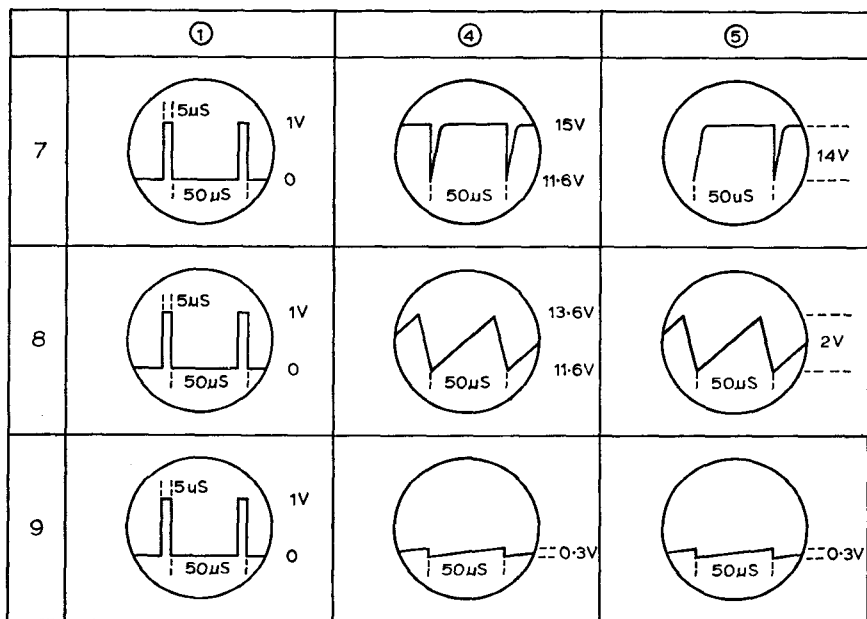
III/6 self-switching timebase

This is another timebase circuit, this time of the 'self-switching' variety as used in oscilloscopes, and giving a linear sweep by the use of negative feedback through the charging capacitor (Miller timebase). Tr1 is the switching stage, Tr2 the linearising stage, Tr3 a buffer, and the operational amplifier IC1 is a switching comparator.
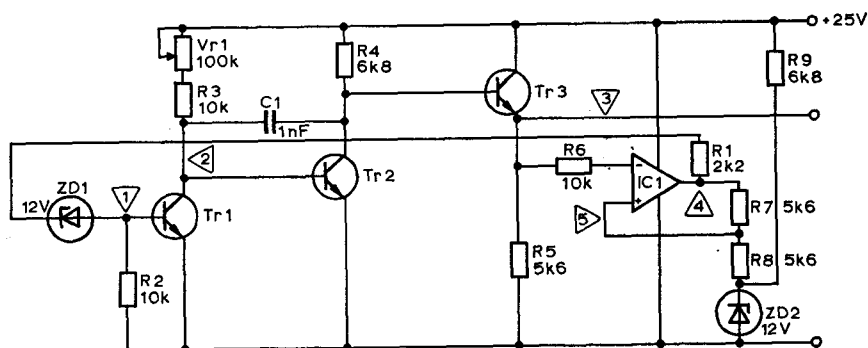
Imagine that Tr1 has just turned off, with the voltage at the collector of Tr2 high. The connection of C1 to the +25V line through R3 and VR1 starts C1 charging when Tr2 starts to conduct. A small rise in voltage at the base of Tr2 will cause a large drop at the collector, which will be fed back as a correcting voltage to the base; so that C1 can only charge linearly, any deviation being corrected by feedback. The effect of this is that the voltage level at the collector of Tr2 falls linearly.

When the voltage at the collector of Tr2 was high, the emitter voltage of Tr3 was also high, holding the voltage level at the − input of the operational amplifier high. This, in turn, made the output of the IC low, and the feedback to the + input of the IC kept the voltage of the + input at a level about half way between 12V (set by zemer diode ZD2) and the output voltage of IC1.

When the decreasing voltage level at the emitter of Tr2 reaches the voltage level of the + input of IC1, the operational amplifier will switch over, with the positive feedback through R7, R8 speeding the switch over. The output of the operational amplifier is now high, and ZD1 conducts, turning on Tr1, ending the linear sweep, and starting flyback. The voltage at the + input of the operational amplifier is now halfway between +12V and +25V, so that the voltage at the emitter of Tr3 must reach this level before the circuit can switch over to start the timing cycle again.

This circuit will oscillate continuously when operation is normal, and no static voltage readings will be of any help unless a fault has caused the action to stop; accordingly, all the voltage readings correspond to fault conditions. The oscilloscope readings, one of which is a normal set, are taken when the circuit is oscillating but in some cases with abnormal outputs.

III/6   Table of Voltage Readings

All readings are for fault conditions.

No.	1	2	3	4	5
1	0	0·6	0·2	24	18
2	0·7	*	0	24	18
3	*	0·6	0·2	24	18
4	0	0·6	0·1	*	*
5	0	*	25	*	12
6	0·7	0·6	11	24	18

*indicates a very low reading.
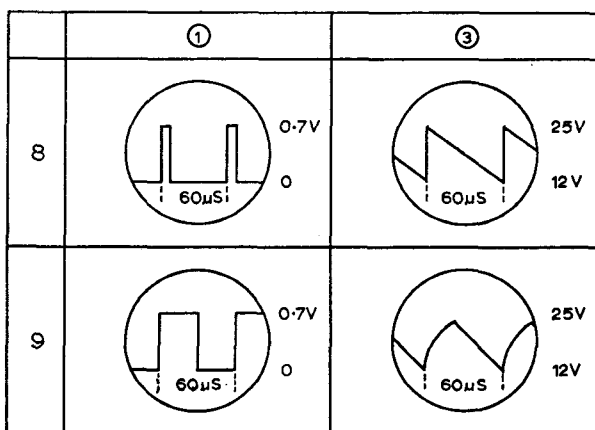
MEASURING CIRCUITS

IV/1 Wheatstone bridge using a 741 operational amplifier

THE TRADITIONAL Wheatstone Bridge circuit is still an excellent method of making precise measurements on resistors, and a modern form of this circuit is illustrated here. A type 741 operational amplifier is used as a level comparator with VR1, a precision ten-turn helipot, used as the ratio measuring device.

The bridge part of the circuit consists of VR1 together with Ry and Rx. Ry is the standard resistor, whose value is selected by the range switch Sw1, and Rx is the unknown value of resistance whose value is to be found. The bridge is said to be balanced when the voltage at the junction of Ry and Rx is equal to the voltage at the slider of the potentiometer. When this condition is fulfilled, the potentiometer ratio, read from a digital dial on the potentiometer, equals Ry/Rx.

The operational amplifier is used to increase the sensitivity of the measurement by applying the voltage at the slider of the potentiometer to the + input, and the voltage at the junction of Ry and Rx to the −input of the operational amplifier. If these voltages were exactly equal, and the null-setting of the operational amplifier correct, then the output of the amplifier would be zero or very close to zero, so that both of the LEDs in the output of the amplifier would be illuminated.

If the voltage at the + input is high, the output voltage of the 741 is also high, so that the LED labelled HIGH goes out, and the LOW LED is on. This instructs the user to change the potentiometer setting to a lower ratio. Conversely, if the + input is low, the output voltage is low and the HIGH LED is lit with the LOW LED extinguished. At balance, both LEDs will be lit, and

the reading of the ratio is taken from the potentiometer dial. This ratio is multiplied by the value of the standard resistor set by the range switch Sw1, giving the value of the resistor Rx.

Before use, the null set potentiometer VR2 is set by closing switch Sw2 and adjusting VR2 so that both LEDs are equally illuminated.

The voltage across the bridge is kept deliberately low by using diodes D1, D2, D3 so that the input voltages are not too far removed from the balanced output voltage of zero, so avoiding amplifier errors due to large 'common mode' inputs.
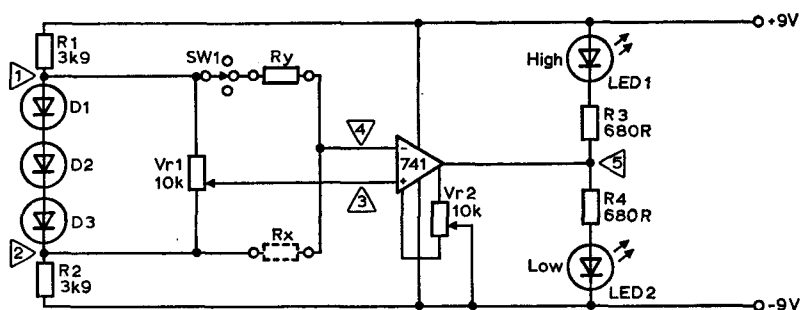
IV/1   Table of Voltage Readings

The tests were carried out using the range for which Ry=1k, and with the value of Rx also 1kΩ.

| No.	1	2	3†	4	5	Lamps High	Low
1	0·8	−0·8	0	0	0	lit	lit
2	1·2	−1·2	0	−1·2	8·5	out	lit
3	1·2	−1·2	0	0	0	lit	lit
4	1·2	−1·2	0	0	*	lit	out
5	−2·2	−4·6	−3·4	−3·4	−3·4	bright	dim
6	1·2	−1·2	0	0	0	out	bright

*indicates a very low reading.
†indicates that a FET voltmeter was used for the readings.

IV/2 voltmeter using op-amp

Before the days of transistors, rather insensitive voltmeters were commonly used, such as the 5V, 5mA full scale instrument featured in this circuit. Such a meter can be made the basis of a sensitive instrument with a high input resistance by the use of a type 741 operational amplifier in the circuit shown.

The meter is connected between the output of the operational amplifier and the zero connection between the two batteries, so that a reading is obtained when the output of the operational amplifier rises above zero. A negative feedback loop consisting of VR2, R5,R4 is connected to the −input, and adjusted so that the gain of the operational amplifier is ×5. VR1 serves as the null adjustment, so that with the input terminals shorted together, the meter can be set to zero.
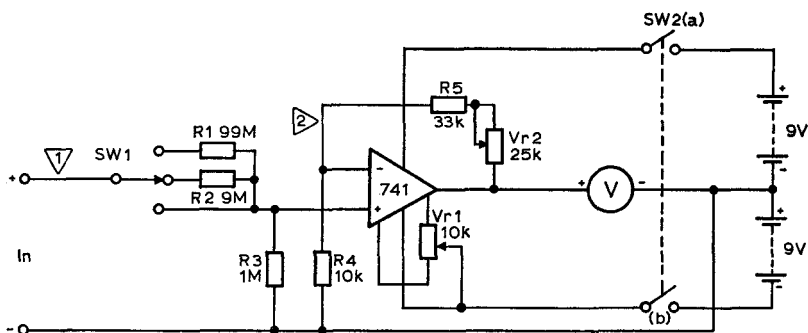
The input is taken to the selector switch, Sw1, selecting the ranges 1V, 10V, 100V for full scale deflection of the meter (which uses the original 0 to 5 dial scale). An input of 1V to the + input of the 741 causes 5V to appear at the output with only a very small error; the gain can be controlled very exactly because of the very high gain of the 741 if the feedback loop is broken.

Because the 741 is acting as a 'follower', with the output in phase with the input, the input resistance is very high, many megohms, and is deliberately limited by using the 1MΩ resistor R3. In this way, a 'figure of merit' of 1MΩ/V is obtained.

Such a meter should be tested on all of its ranges, and the readings of the meter itself can be used in diagnosis, In the table, one set of readings is normal, the others represent fault conditions.

IV/2 Table of Voltage Readings

No.	1	range set	2	meter reading
1	1·0	C	0	0
2	10	B	0·4*	2
3	100	A	0·8*	4
4	1·0	C	1·0*	5
5	1·0	C	1·0*	4
6	1·5	A	1·0*	5

*indicates an approximate reading; the true reading might be slightly more or less.

IV/3 voltmeter using MOS device

The new generation of MOS operational amplifiers makes the design of high input resistance voltmeters even easier, as balanced power supplies are no longer needed. One other merit of the MOS devices is that zero voltage in can give zero voltage out, even with a single-ended supply, so that voltmeter circuits of the type illustrated can be built.

This uses a type CA3130 MOS operational amplifier with a single 9V supply to drive a 1mA meter through a series resistor chain R11, VR2. Voltage ranges from 0·01 to 100V full scale are covered by a combination of input switched attenuator and negative feedback switching. Once again, VR1 is a null potentiometer adjusted so that the milliammeter reading is zero with the input terminals shorted.

An input on the correct range setting will be applied to the + input of the operational amplifier (maximum input 1V in this circuit), and the output voltage will be at a level which will cause the − input voltage to equal the

+ input voltage, due to the very high gain of the amplifier. On ranges A and C, the − input will reach a maximum of 1V; on ranges B and D a maximum of 0·1V, and on range E a maximum of 0·01V. For each of these, the feedback used will ensure that the voltage at the output pin will be 1·0V, and the preset meter resistor VR2 will be set so that the meter reads full scale for 1V at the amplifier output.

The input resistance of the operational amplifier is extremely high, measured in Tera-ohms ($1T\Omega = 10^{12}\Omega$), and decoupling of the input resistance R3 by capacitor C1 is needed to avoid the pickup of r.f., a.f., and hum.

The table of values, one set of which is normal, shows the voltages applied, the range selected, and the meter readings on the 1mA meter, along with voltage readings taken with another meter at a few points where such readings can be taken.
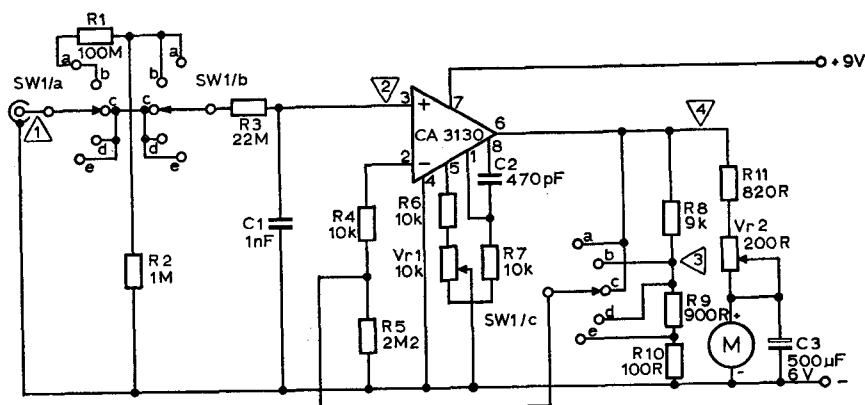
IV/3   Table of Voltage Readings

No.	1	range	2	3	4	meter reading (0 to 1)
1	10	B	0·1	0·1	0·8	0·8
2	1·0	C	1·0	0·1	1·0	1·0
3	0·1	D	0·1	0·1	1·0	0·9
4	1·0	C	0	0·9	9·0	end stop past 1·0
5	0	C	0·1	0·01	0·1	0·1
6	100	A	1·0	0·1	1·0	0

IV/4 temperature change indicator

Many industrial processes are temperature sensitive, but the exact measurement of temperature is less important than the indication of changes of temperature. The circuit shows a temperature change indicator using a thermistor Th1 in a bridge circuit. The bridge voltage is kept low by feeding the bridge arms through the limiting resistors R6,R7, and the range of settings is limited by the resistors R2, R3, on each side of the range potentiometer VR1. Since this potentiometer can also be used to set the output to zero, the usual null adjusting potentiometer used in this type of circuit is omitted.

In use, the thermistor is connected so as to monitor the temperature which is
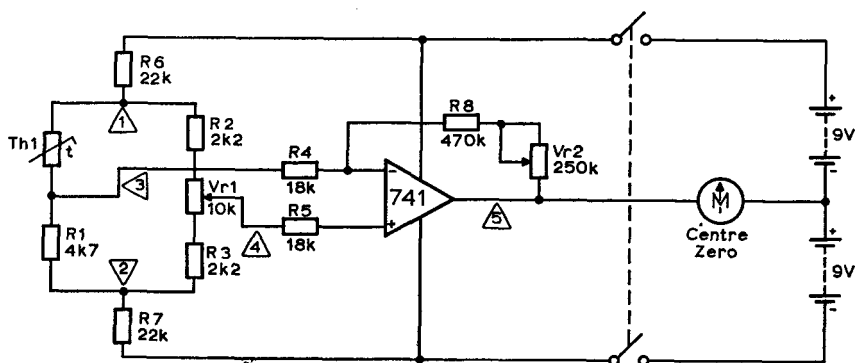
IV/4   Table of Voltage Readings

A zero reading in this set of readings may correspond to a very small value which cannot be read by the multimeter.

No.	1	2	3	4	5
1	—4·4	—5·4	—4·9	—4·9	—4·9*
2	1·1	—1·1	0	0	0
3	1·1	—1·1	0	—1·1	—8·6
4	2·2	—2·2	—2·2	0	8·6
5	1·1	—1·1	0	0	varies
6	1·6	—1·6	0	—1·6	—8·6
7	In this fault condition, readings seem normal, but the circuit is much too sensitive to small temperature changes.				

*indicates an approximate reading.

to be checked, and the potentiometer is set to give a zero output on the centre-zero meter at normal temperature. Potentiometer VR2 adjusts the sensitivity of the circuit, so that the meter does not deflect excessively for very small changes in temperature. The voltage to each of the 741 inputs should now be zero, and the output voltage also zero, with the bridge balanced.

Any change of temperature will cause a change of resistance of the thermistor so changing the balance of the bridge and causing a meter reading which will indicate whether the temperature has risen or fallen.

One of the sets of readings is normal, with the thermistor temporarily replaced by a resistor whose resistance value is the same as that of the thermistor at the normally-set temperature. Note that a zero reading may simply mean a very low voltage which cannot be read by a conventional multimeter.

IV/5 incident light meter using a photoconductive cell

The measurement of incident light is now an important part of industrial practice, since legally specified minimum standards of illumination are now enforced. This circuit is of an incident light meter using a photoconductive cell. Since the range of values of incident light is very large, the instrument has been designed to use a non-linear scale, so that some form of calibration would be needed, using a spot photometer, or a calibrated light source.

The LDR (light dependent resistor) is fed from a series chain of diodes whose V/I characteristics are approximately logarithmic in the range of
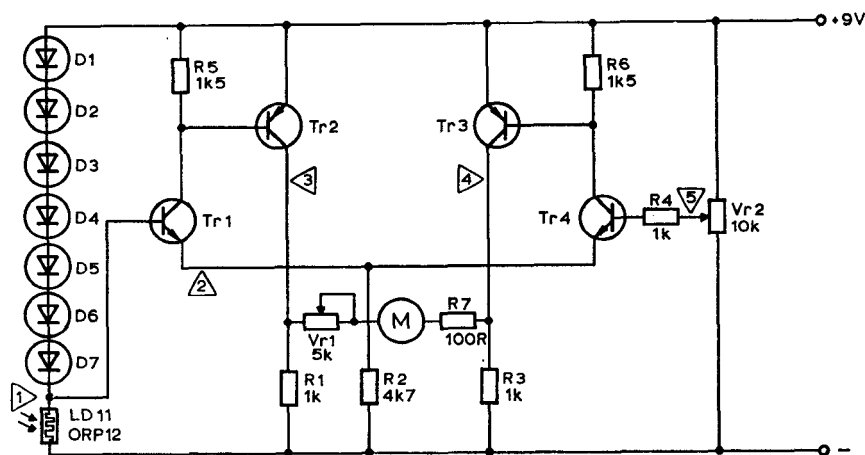
values used. This means that the current passed by the diodes is approximately proportional to the logarithm of the voltage across them over a small range of voltage values. In this way, a large change of resistance of the LDR does not cause a very large change in the voltage across it, since the current through the diodes will change.

The voltage across the LDR is applied to the base of Tr1, the first stage of a balanced d.c. amplifier whose zero setting is obtained by adjusting VR2. The current in the collector of Tr1 is used to apply a bias to the base of Tr2, and the output is taken across a 1kΩ load resistor in the collector circuit of Tr2. The bridge connection of the meter makes the reading unaffected to a great extent by variations in the supply voltage, and the range of the meter is set by VR1.

In practice, VR2 would be used to set the meter to zero for the lowest illumination level, and VR1 to set the meter to maximum reading for the brightest illumination to be measured.

The sets of readings, one of which is normal, are taken with fixed illumination on the LDR. The meter is then adjusted to zero by setting VR2, and readings taken. For some fault conditions, it may be impossible to adjust to a zero output on the meter; in such cases, VR2 has been set half-way along its track.

IV/5   Table of Voltage Readings

No.	1	2	3	4	5
1	4·8	4·2	6	6	4·8
2*	3·8	3·8	8·8	2·4	3·8
3	3·8	3·3	0	0	3·8
4	3·8	3·2	2	2	3·8
5	3·8	3·2	2	0·6	3·8
6	4·6	4·0	2·5	2·5	4·6

*in this fault, the meter cannot be set to zero.

IV/6 direct-reading capacitance meter

Bridge readings of capacitance are always rather tedious to make if a large number of capacitors have to be tested, and a direct-reading capacitance meter, using a meter dial reading, is very useful. The circuit illustrated is of a simplified version, which though limited in range due to its rather low sensitivity is nevertheless very useful.

The CMOS gates IC1 to IC4 are wired as a multivibrator and buffer amplifier, with four of the inputs taken to $+9V$ through $220k\Omega$ resistors to keep these inputs high. The wave time is set by R9,C3, and R9 has been adjusted in this circuit so that the squarewave output from IC1 is exactly 1mS in duration. The two portions of the wave will not usually be identical, and the values are not exactly predictable because of the variation in characteristics from one CMOS gate to another.

The squarewave output, which has very rapid rise and fall times, is used to switch the transistors Tr1 and Tr2. During the positive-going excursion of the wave, Tr1 is on, and the capacitor Cx which is being measured is charged rapidly to the voltage, 10V or 1V, set by Sw1. During the negative excursion of the squarewave, Tr1 is off, and Tr2 is on, discharging Cx through the $100\mu A$ meter M, which can be shunted by R3 to make its full-scale deflection current equal to 1mA.

Since the capacitor is being discharged through M 1000 times per second, the meter reading will be steady, as the movement cannot follow such rapid changes, and the current indicated on the meter is the average amount of charge flowing per second. The charge on a capacitor C charged to voltage V is CV coulombs, so that the current reading on the meter is 1000CV, with C in Farads, and V in volts.

Three ranges are used: 0–5nF, 0–50nF, 0–500nF. The main source of error is the incomplete discharge of Cx because of the voltage across Tr2; commercial instruments use MOSFETs in a bridge circuit to minimise this effect; higher supply voltages are also helpful.
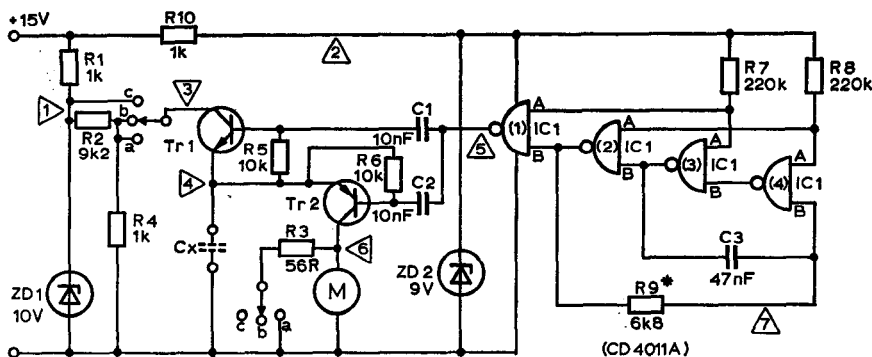
IV/6   Table of Voltage Readings

In this circuit, steady readings are obtained only when a fault is present, so all of the readings below represent fault conditions.

No.	1	2	3	4	5
1	3	9	3	Oscillating	
2	10	9	10	0	Oscillating
3	10	9	0	0	Oscillating
4	10	9	10	5	Oscillating
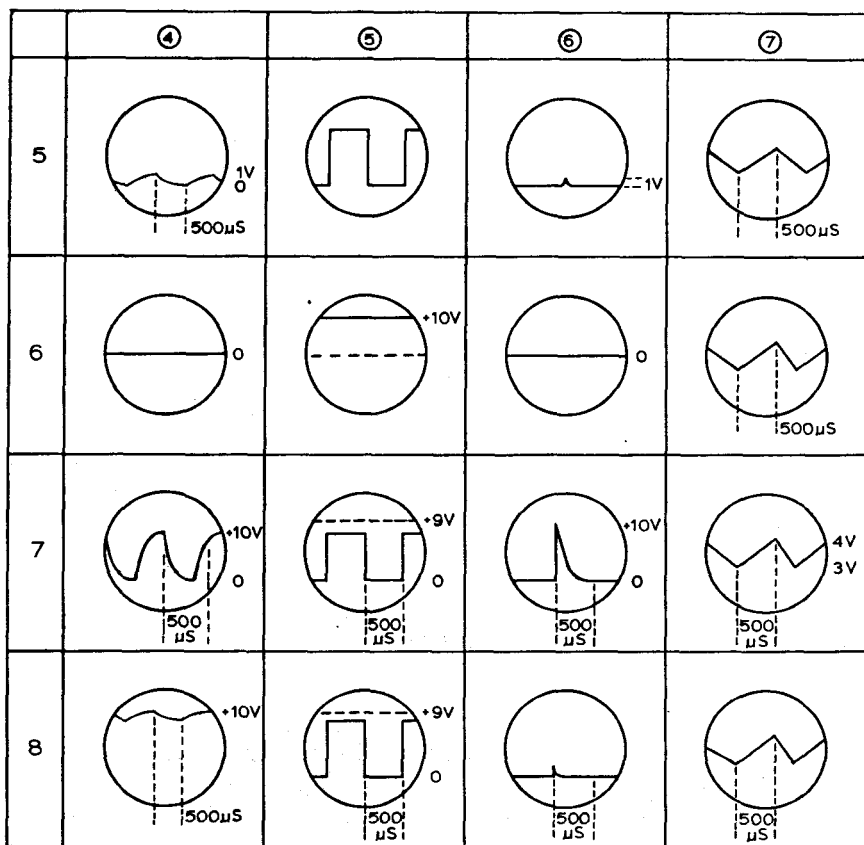
SECTION V

OSCILLATORS

V/1 oscillator providing a sinewave output

THE OSCILLATOR circuit shown here is intended to provide a sinewave output at a frequency of about 180kHz. The oscillator uses LC tuning, but the capacitor is placed in series with the winding of the transformer rather than in parallel with the winding connected to the collector as is more usual. The oscillator in this particular example is very easily upset by changes in bias conditions or supply voltage, and in most of the fault conditions noted no oscillation is detected.

The transformer is connected so that the current in the base winding is in phase with the current in the collector winding, and the transistor is biased to linear operation by resistors R1 and R2. Bias stabilisation is assisted by R3, decoupled by C2. To reduce the effect of a load on the circuit, the output is taken from a separate winding of a small number of turns, so that the output is a low-amplitude signal at low impedance.

It is worth noting that, though normal-looking voltage readings can be obtained from this circuit while it is oscillating normally, the voltage readings can appear very odd when the bias is incorrect and the action non-linear. The reason is that the circuit may oscillate with the transistor cut off for part of the cycle.

Since the meter voltages measured are average voltages, false readings will be obtained because of the rectifying effect of the transistor when operated partly cut off. The same applies when the transistor is saturated for part of the cycle. Assume in this case that one set of readings corresponds to normal linear sinewave working, and the other readings correspond to zero-output fault conditions.

V/1 Table of Voltage Readings

No.	1	2	3	4
1	0·8	0	8·0	0·8
2	1·0	0·4	9·0	1·0
3	0·2	0·2	9·0	0·2
4	0·3	0	9·0	0
5	1·0	0·4	0	1·0

6   All voltages normal, but no trace of oscillation.
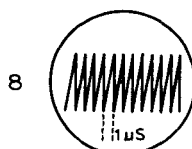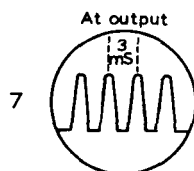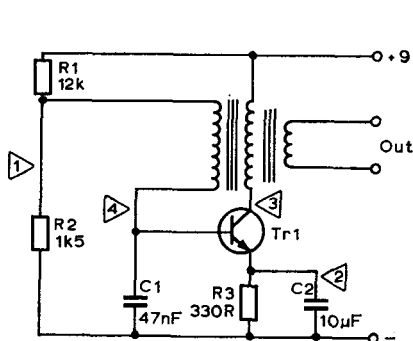
V/2 phase-shift oscillator

The circuit is of a phase shift oscillator working at audio frequency. The output from the collector is phase shifted by C1R4, C2R3, C3 and R1,R2, with a phase shift of about 60° in each step, so that the overall phase shift is 180°, which is one of the requirements for oscillation.

The other requirement for oscillation is that the gain of the transistor pair should be just greater than the loss round the phase-shift circuit. This can be achieved using a single transistor. but very often needs selected transistors

for the gain required. A 'superalpha' or 'Darlington' pair, as shown here, has the advantage that higher values of resistors can be used for bias, since the input resistance is much higher than that of a single transistor. Note that the bias resistors R1, R2 are in parallel as far as the signal is concerned, since each is returned to a line at signal earth. The values have been selected to make their combined resistance in parallel equal to the 15kΩ of R3,R4.

Bias stabilisation is assisted by using R8, which has to be decoupled by C4 to keep the gain high. Tr2 is also run at a current of several mA so that the phase shift circuit can be driven from a low impedance.

The waveshape of the oscillation is affected greatly by bias and by overall gain, so that feedback stabilisation of gain is usually used in this circuit, with the feedback loop containing thermistors or similar non-linear elements. Such circuits make voltage readings liable to change in an unpredictable way, so that the simple circuit is considered here. Assume that the normal oscillation is a reasonable sinewave, and that the normal transistor operating conditions will be found when the circuit is operating normally.
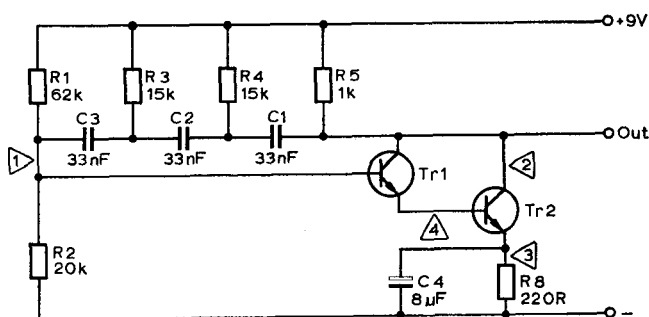
V/2   Table of Voltage Readings

No.	1	2	3	4
1	1·4	0·2	0	0·7
2	1·3	8·5	*	0·7
3	2·2	0·8	1·0	1·6
4	2·2	4·5	1·0	1·6
5	0·5	8·5	*	0·5
6 All voltages normal, but no oscillation.				

*indicates a very low reading.

V/3 crystal-controlled oscillator

When the frequency of an oscillator must be controlled very precisely, a quartz crystal is used as the resonating circuit. The crystal may be used as a series resonant or a parallel resonant circuit, though at different frequencies. The circuit shown here uses a crystal as if it were an inductor in series with a capacitor in an oscillator which provides a sinewave of excellent stability and good waveform.

The oscillation is caused by feedback from the collector circuit of a transistor to its emitter, using the crystal as a filter which passes only the frequency of resonance of the crystal. Tr1 is the amplifying stage, with Tr2 used as a buffer presenting a high impedance to the collector of Tr1 and driving the crystal from the low impedance of its emitter circuit. The emitter circuit of the buffer
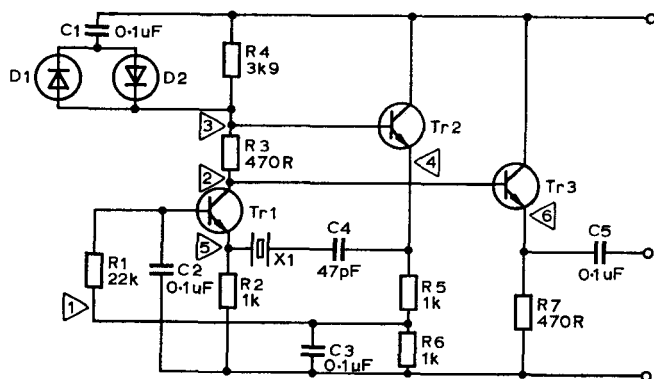
V/3 Table of Voltage Readings

| No.	1	2	3	4	5	6
1	0·25	1·1	1·1	0·5	0	1·1
2	2·3	4·4	5·3	4·6	1·7	3·7
3	1·1	1·9	2·2	2·2	0·5	0
4	1·0	2·45	2·65	2·1	0·4	1·85
5	1·0	0·6	2·7	2·1	0·4	*
6	4·1	8·7	9·0	8·3	0	8·0

*indicates a very low reading.

stage is also used to provide bias for Tr1 through R1 with C3 decoupling the bias supply.

To avoid driving too much signal current through the crystal, the signal amplitude to the base of Tr2 is limited by the diodes D1,D2 which are returned to the positive (but signal earth) line through C1. To avoid loading the oscillating circuits by the output, Tr3 is used as a buffer stage.

The limiting action of the diodes ensures that the amplitude of the sinewave will not overload any of the transistor stages so that the voltage readings taken with the circuit oscillating normally correspond to the readings which would be found in linear stages.

In the table, one set of readings is normal, the others represent fault conditions. The oscillogram represents a fault condition which causes abnormal readings in some parts of the circuit.

At point ③

10 V

200 nS
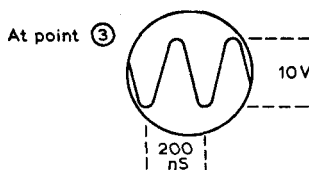
V/4 multivibrator using a 555 timer, with adjustment of duty cycle

The standard design of multivibrator provides a wave in which the ON time is roughly equal to the OFF time (50% duty cycle) when the bias resistors and capacitors are of equal value. The duty cycle can be changed to some extent by changing one time constant, but the frequency is also affected. Using a 555 timer in a multivibrator circuit, as shown here, makes possible the adjustment of duty cycle over a very wide range with little effect on the frequency.

The 555 timer is connected in the usual way for oscillation, with the trigger and timing pins (2 and 6) connected together and taken to the charging capacitor C1. The discharge connection (7) is taken through R2 to one side of VR1, the duty cycle potentiometer, whose slider is connected to C1, and then through R1 to the switching transistors Tr1 and Tr2.

The action is as follows. Imagine that timing has started because the voltage at pin 2 has fallen below 4V ($\frac{1}{3} \times 12$V). The output has gone high, so that Tr2 is on and has switched Tr1 on. Charging current now flows through Tr1, R1 and part of VR1 into the capacitor C1; this times the ON part of the cycle. When the voltage across C1 reaches $\frac{2}{3} \times$ supply voltage (8V in this example), the connection to pin 6 ensures that the 555 switches over, so that pin 7 is

earthed and pin 3 (the output) goes low, cutting off Tr2 and Tr1. C1 now dis-charges into pin 7 through the other part of VR1 and R2, and this times the OFF part of the cycle. By setting VR1 at the end of its track nearest R2, the charging resistance can be high (500k Ω or so) and the discharge resistance low; the opposite is true when VR1 is set to the other end of its track, but the total resistance in the circuit is unchanged so that the frequency is constant.

In the design shown, the minimum time on or off is about 18µS and the maximum about 1645µS, with an operating frequency of around 600Hz.

Since this is an oscillating circuit which is non-linear in action, steady read-ings will be obtained only under fault conditions.
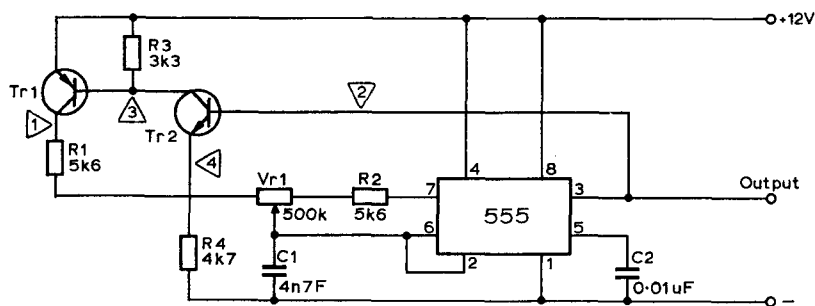
Taken at point ②
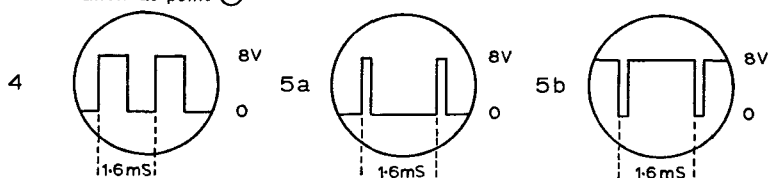
V/4   Table of Voltage Readings

Steady readings are found only when fault conditions exist, so that all the values shown are for fault conditions.

No.	1	2	3	4
1	0	11·7	12	0
2	12	7·8	7·1	6·9
3	0	7·8	7·1	6·9

V/5 multivibrator providing a squarewave output

This is a fairly standard form of the multivibrator circuit which is used to provide a squarewave which can be synchronised if necessary by a signal into either base circuit. The output is used, after differentiation and polarity selection, as a timing pulse. In action, imagine that Tr1 has just switched on, drawing current so that its collector is bottomed. The coupling by C1 to the base of Tr2 ensures that this base voltage has been driven down by about 9V as Tr1 switched on, so that Tr2 is off, and its collector voltage is high, keeping Tr1 on.

Because the base of Tr2 is returned to +9V through R3, C1 will charge up so that the base voltage of Tr2 rises steadily towards +9V. At a base voltage of about 0·6V, Tr2 will start to draw current, and the voltage at its collector will drop, pulling down the voltage at the base of Tr1 because of the coupling through C2. This causes the voltage at the collector of Tr1 to rise, and because the two transistors act as a high-gain amplifier with positive feedback, Tr2 switches off rapidly, and Tr1 switches on rapidly. The waveform at the collector of Tr1 does not rise very rapidly, because one side of C1 is held at the 0·6V level by the base of Tr2, and the other connection charges through R1.
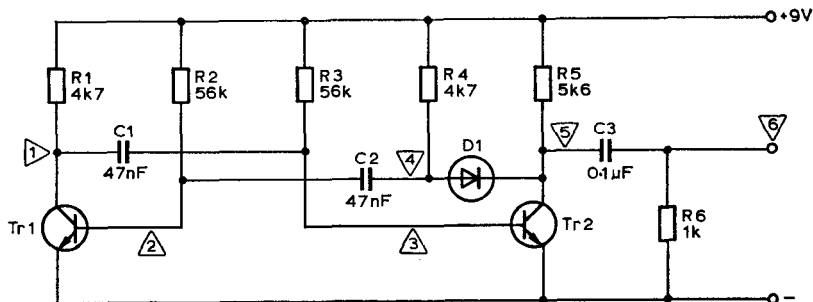
The voltage drop at the collector of Tr2 is very rapid, however. When the opposite action is caused by the charging of C2, the collector voltage of Tr2 can rise quickly as the diode D1 cuts off, leaving C2 to be charged through R4. The output at this collector is therefore a squarewave with fast falling and rising edges. The circuit is not sensitive to supply voltage changes, and will oscillate at supply voltages as low as 1·5V.

Voltage readings on this circuit when it is oscillating are not particularly useful because of the effect on the meter of the average values of the signal, so that all the values in the table refer to voltages found in fault conditions

which have caused the oscillation to stop. The oscillograms show one set of normal traces and three fault conditions in which oscillation has continued but the waveform is abnormal.

V/5 Table of Voltage Readings

All of the readings are for fault conditions, since steady readings are found only under some fault conditions.

No.	1	2	3	4	5
1	9·0	*	0·6	1·0	0·2
2	0·2	0·6	0·6	9·0	0·2
3	0·2	0·6	*	9·0	9·0

*indicates a very low reading.
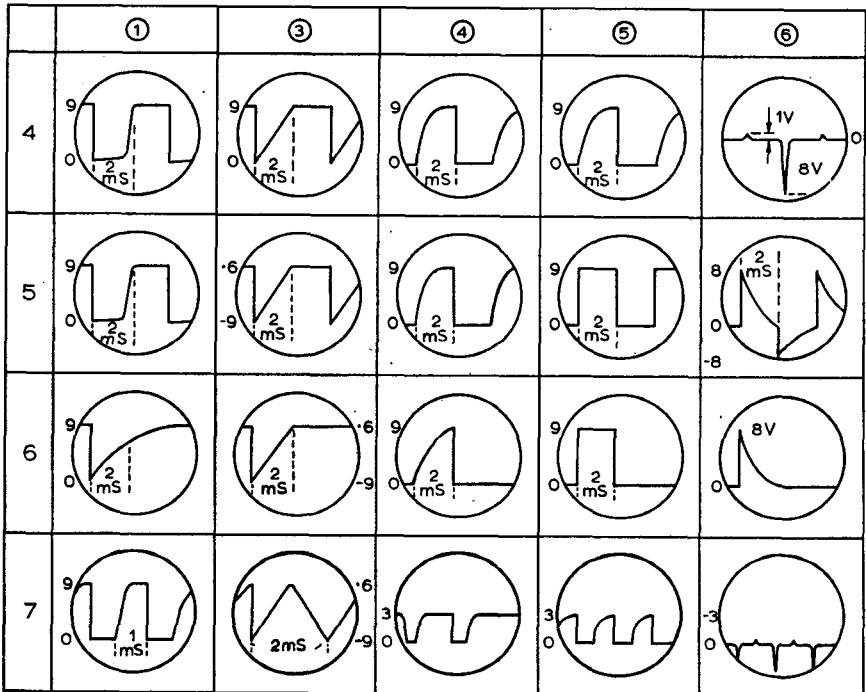
V/6 multivibrator circuit with steep sided output waveform

There is a great variety of multivibrator circuits, each with special advantages and disadvantages. The circuit shown here draws current from the supply for only half of its cycle, so that the current drain can be small, but the supply must be thoroughly decoupled from any other circuits; in addition, the timing is affected by any trace of hum on the supply, which causes severe jittering. Its advantages are that the output wave is steep-sided and that the circuit will keep oscillating even if the values of the components change very considerably.

To follow the action, imagine that Tr1 has just started conducting and Tr2 is off. The switch-on of Tr1 is rapid because of the connection of its base through C2 to the collector of Tr2, so that the rise in voltage at this collector aids the switch-on of Tr1. At the same time, the sudden rise in voltage is communicated to the emitter of Tr2 through C3, the timing capacitor, which then charges by passing current through R4 to earth.

During this time, Tr2 is held off by the positive voltage on the emitter, since its base voltage cannot change rapidly because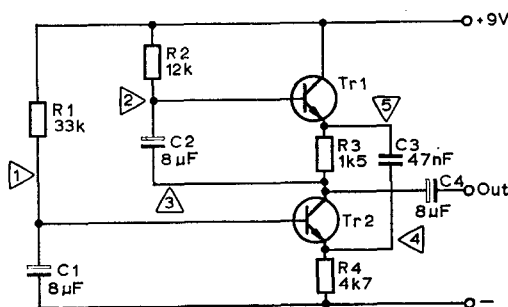 of C1. As C3 discharges Tr2 will eventually switch on, so that the voltage at its collector drops, causing the base voltage of R1 to drop because of the coupling through C2. With Tr1 off, C3 now discharges through R3 and supplies the collector current of Tr2; only the bias current of Tr2 is being supplied by the 9V line during this part of the cycle. The discharge continues until the voltage at the emitter of Tr1 drops sufficiently to allow conduction to start again, when the cycle repeats.

In the table of voltage readings, the normal reading set has been marked, because measurements taken on this type of oscillating circuit can be very misleading. Note in particular that the emitter voltage of Tr2 seems to be higher than that of its base; this is because base voltage is fairly steady during the cycle, but the emitter voltage is high, with Tr2 cut off, for about half the cycle.

V/6   Table of Voltage Readings

The normal set has been marked, since this is an oscillating circuit in which the values found do not resemble these in linear stages.

No.	1	2	3	4	5	
1	3·8	7·1	6·1	4·2	7·2	NORMAL SET
2	0	8·6	8·5	0	8·6	Not oscillating
3	3·6	3·2	3·2	3·0	3·1	Not oscillating
4	2·9	7·8	3·4	2·6	8·1	Oscillating
5	2·6	7·6	6·6	3·4	7·5	Oscillating
6	2·8	4·8	4·6	3·0	5·0	Oscillating

Taken at output terminal
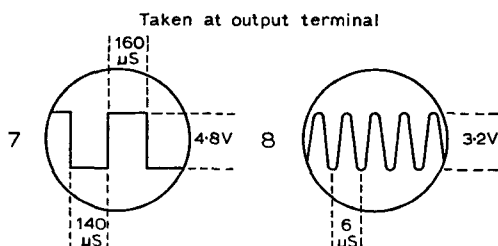
TRIGGER CIRCUITS

VI/1 Schmitt trigger circuit

THE SCHMITT trigger is the most basic two-transistor trigger circuit, and this example of the circuit is fairly typical of the type. With no input, transistor Tr2 is held on by the connection of its base to the 9V line through R2, though the voltage to which the base can rise is limited by connecting R3 to earth. With Tr2 saturated, the voltage across R4 is enough to hold Tr1 cut off, even when the base of Tr1 is positive.

As the voltage at the base of Tr1 is raised, however, a level will be reached at which Tr1 will start to conduct, and the circuit then acts as a high-gain amplifier with positive feedback. The current flowing in Tr1 causes the base voltage of Tr2 to drop, switching current from Tr2 into Tr1 which rapidly saturates, holding Tr2 cut off by the high voltage at its emitter and low voltage at the base.

As the switchover is very fast, this circuit is ideal for making a steep rising
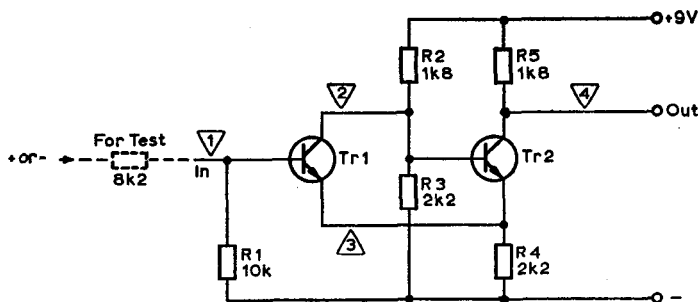
waveform from a slowly rising one. In addition, the circuit has trigger hysteresis, meaning that once a voltage level has triggered the circuit, a lower voltage level is needed to trigger the return to the original conditions. The difference between these two levels is called the hysteresis voltage, and it can be used to ensure that noise or other disturbance at the input does not cause false triggering or jitter.

In the circuit shown, the voltage readings are taken for the two conditions, high and low input voltage. For the low input tests, an $8 \cdot 2k\,\Omega$ input resistor is connected to the negative line. For high input, the $8 \cdot 2k\,\Omega$ resistor is returned to the positive line.

VI/1   Table of Voltage Readings

Each set of readings has been taken with the input LOW (earthed) and again with the input HIGH (to V+ through $8 \cdot 2k\,\Omega$)

No.	HIGH/ LOW	1	2	3	4
1	HIGH	4·4	5·0	4·4	5·3
	LOW	2·9	3·5	3·9	4·6
2	HIGH	4·0	3·4	3·4	8·2
	LOW	1·6	1·0	1·0	8·2
3	HIGH	4·2	3·7	3·6	9·0
	LOW	0	5·2	0	9·0
4	HIGH	4·6	4·6	3·5	9·0
	LOW	0	3·7	3·1	5·2
5	HIGH	2·0	1·4	1·4	9·0
	LOW	0	1·0	0·4	8·8
6	HIGH	4·6	6·6	6·0	6·1
	LOW	0	6·6	6·0	6·1

VI/2 trigger circuit using an IC

Very sensitive trigger circuits can be made using integrated circuit operational amplifiers, and some ICs are specifically designed for trigger operation, in which case they are usually called threshold detectors. The circuit shown here is of a very sensitive trigger circuit intended to produce steep-sided pulses from a sinewave or other input at a low level.

The input wave is clipped by R1 and diodes D1,D2, and then coupled by C2 to the gate of the n-channel FET, Tr1. This FET is biased through a 1M Ω resistor R2 from the emitter of Tr3, which also biases the + input of the operational amplifier/threshold detector. The base of Tr3 is held at a fixed voltage by R5, R6, so that the voltage at the emitter is stabilised.
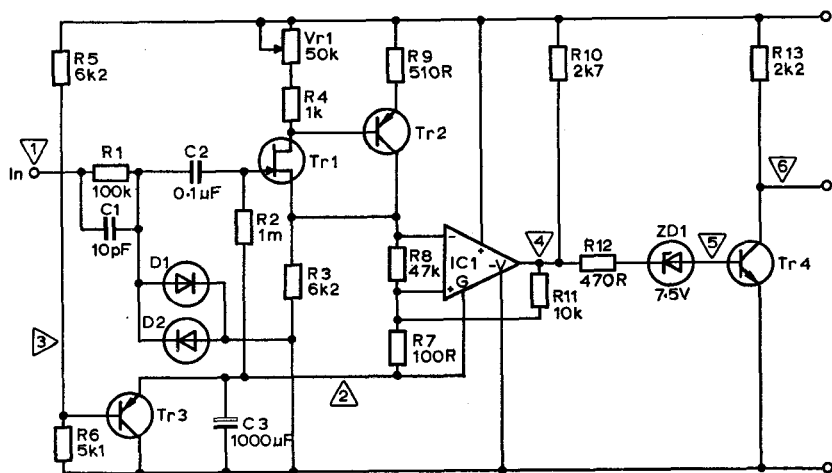
Tr1 is coupled to Tr2 to form a negative feedback loop, with Tr2 providing current gain, and biasing the negative input of the operational amplifier. The exact value of bias at this input is set by the variable VR1, which controls the voltage level at the base of Tr2. The output of the IC, which will be 12V or 6V according to which way it has been triggered, is partly fed back to the + input through R11, and applied through R12 and ZD1 to the base of Tr4, which acts as a level changing transistor stage, so that the output pulse levels are 0.5V and 12V.

The current in the IC which flows into the emitter of Tr3 is about 10mA.

In normal use, the V+ supply would be +6V, and the V− supply would be −6V.

In the table of readings, the voltage levels have been taken just after a positive input pulse (High) or just after a negative input pulse (Low). One set of readings is normal for this circuit, the others represent fault conditions.

VI/2 Table of Voltage Readings

The readings have been taken just after a positive-going pulse (HI) and again just after a negative-going pulse (LO).

No.	HI/LO	1	2	3	4	5	6
1	HI	11*	11	11	12	0·7	0·5
	LO	11*	11	11	12	0·7	0·5
2	HI	6·0	6·0	5·4	6	0	12
	LO	6·0	6·0	5·4	12	0·6	0·5
3	HI	0·7	6·0	5·4	12	0·6	0·5
	LO	0·7	6·0	5·4	12	0·6	0·5
4	HI	1·8	6·0	5·4	12	0·6	0·5
	LO	1·8	6·0	5·4	12	0·6	0·5
5	HI	6·0	6·0	5·4	6	0	12
	LO	6·0	6·0	5·4	12	0	12
6	HI	10	10	9·6	12	0·6	0·5
	LO	10	10	9·4	12	0·6	0·5

*indicates an approximate reading.

VI/3 trigger circuit using a triac

Trigger circuits are very commonly found in power control circuits using triacs or thyristors, and this is an example of such a circuit. The supply voltage is applied to the emitter of a p-n-p transistor, which is then switched by full-wave rectified pulses at 100Hz applied to its base. The amplitude of the pulses is such that the transistor Tr1 is saturated except for the short time when the input a.c. waveform crosses the zero level, so that the output waveform at the collector of Tr1 is a series of narrow negative-going pulses which are then applied after attenuation by R3,R4 to the gate of the SCS (silicon-controlled switch). This latter device will conduct heavily when the gate electrode voltage is negative with respect to the anode voltage.

The anode of the SCS is fed from the capacitor C1, which can be charged slowly through R5, or more quickly through Tr2 and R6. The base of Tr2 is returned to the temperature measuring circuit R7,VR1,Th1, so that the voltage at the base of Tr2 depends on the setting of VR1 and the temperature at the thermistor.

Imagine C1 discharged. Charging will take place rapidly through Tr2 until the voltage set by the thyristor and VR1 is reached, and then charging will continue slowly through R5 until the negative pulse at the collector of Tr1 causes the SCS to fire, discharging C1 through the opto-coupler, which consists of a light-emitting diode facing a phototransistor in a sealed package. In this way the trigger circuits can be kept isolated from the triac circuit, avoiding earthing problems. Depending on the setting of VR1 and the temperature at the thermistor, the capacitor C1 may charge very slowly, providing enough

VI/3 Table of Voltage Readings

Two sets of readings have been taken in each case, one with VR1 at maximum setting (MAX) and the other with VR1 at minimum setting (MIN).

No.	SETTING	1	2	3*	4*	5
1	MAX	15	0	0	0	0
	MIN	15	0	0	0	0
2	MAX	14·4	14·4	7·2	0	14·4
	MIN	14·4	14·4	7·2	0	0·6
3	MAX	14·4	14·4	7·2	14·4	14·4
	MIN	14·4	14·4	7·2	14·4	14·4
4	MAX	14·4	14·4	7·2	slow oscillation	
	MIN	14·4	14·4	7·2	rapid oscillation	
5	MAX	14·4	14·4	7·2	rapid oscillation	14·4
	MIN	14·4	14·4	7·2	rapid oscillation	14·4

*indicates readings made with a FET voltmeter.
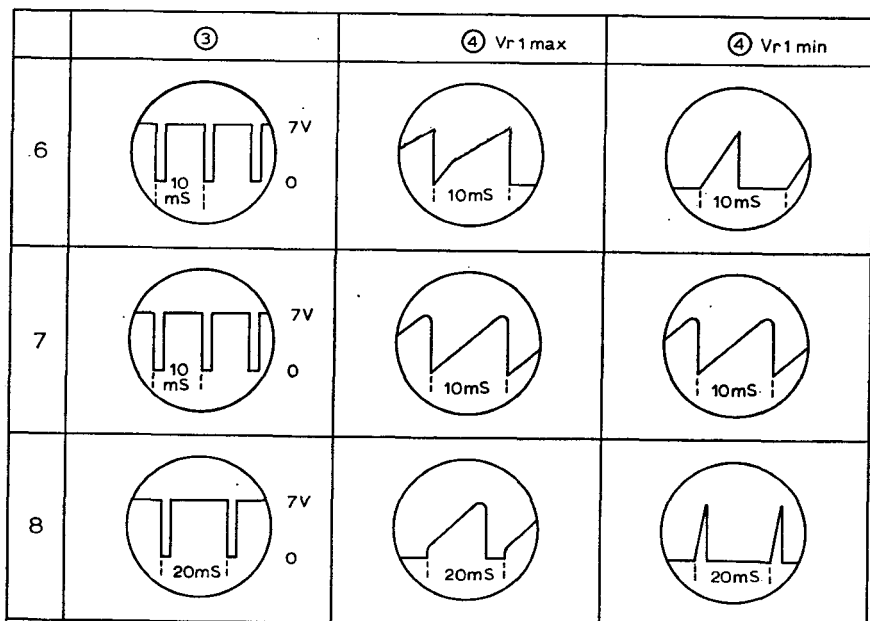
energy to fire the triac circuit only occasionally, or it may charge rapidly, causing the anode of the SCS to exceed gate voltage before the negative pulse occurs, and so firing the triac early in the cycle and so applying more power in the triac circuit.

The readings shown are taken with a steady 12·3V applied to the input, and with VR1 alternately at its maximum and minimum settings. One set of readings is normal, the others represent fault conditions.

VI/4 IC trigger ciruit using discrete transistors

This is a much more elaborate trigger circuit; it is in fact the internal circuitry of an integrated circuit trigger circuit; but we can make up the circuit in discrete form as shown.

Resistors R3,R4 set a reference voltage level which can be monitored or adjusted at the V Ref pin. The reference voltage is applied to the base of Tr5 through R2, and this point is also connected to the collector of Tr6. If the voltage at the input of the circuit is low, Tr1 is cut off, Tr3 is cut off, and the
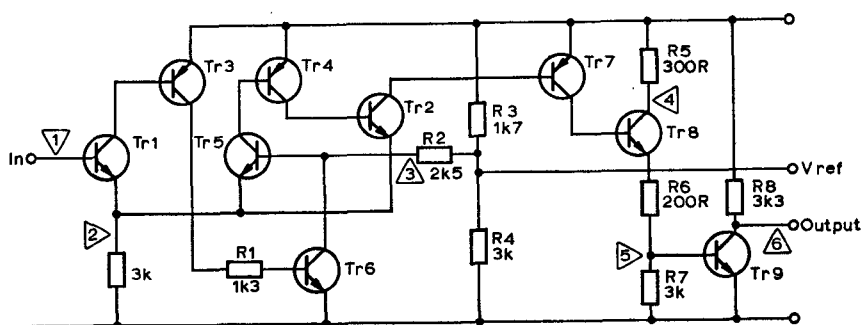
base of Tr6 is low, allowing the reference voltage at the base of Tr5 to control current through Tr4, Tr5, and R5. The base-emitter current of Tr4 causes current to flow in Tr2, Tr7, Tr8 and Tr9, so that the output, which uses an external load resistor, is low.

If the input voltage is greater than the reference voltage, Tr1 conducts

through Tr3, and Tr6 conducts, short circuiting the base of Tr5 to earth. This cuts off the transistors Tr2, Tr7, Tr8, Tr9 so that the output voltage rises.

With the circuit built using separate transistors, the voltage readings can be taken anywhere in the circuit, and six points have been chosen. Two sets of readings are made at each point, one HIGH, with the input voltage above the level of the reference voltage, and one LOW, with the input voltage below the level of the reference voltage. One set of readings is normal, the others represent fault conditions.

VI/4 Table of Voltage Readings

Two sets of readings are taken for each case, one with the input high (HI) at +4V, the other with the input low (LO) at 3·0V.

| No.	HI/LO 1	2	3	4	5	6
1	HI	3·6	3·2	5·0	0	5·0
	LO	2·6	3·2	2·7	0·6	0·6
2	HI	3·6	*	5·0	0	5·0
	LO	2·6	3·2	2·7	0·6	0·6
3	HI	3·6	*	5·0	0	5·0
	LO	2·6	3·2	2·0	0	5·0
4	HI	3·6	*	5·0	0	5·0
	LO	2·6	3·2	5·0	0	5·0
5	HI	3·9	4·5	2·7	0·6	0·6
	LO	3·9	4·5	2·7	0·6	0·6
6	HI	3·6	3·6	5·0	0	5·0
	LO	2·6	2·6	5·0	0	5·0

*indicates a very low reading.

CONTROL & INTERFACE CIRCUITS

VII/1 sine-to-squarewave converter

THE CIRCUIT here is a sine-to-squarewave converter, used wherever a sinewave is generated to take advantage of the stability of sinewave generators, but a squarewave is needed for timing purposes. Note that the transistors used in this circuit are both p-n-p types so that the bases must be made negative with respect to the emitters to switch the transistors on.

When a 10V peak-to-peak sinewave is applied at the input, the positive going portion is clipped by the diode D1, which will conduct when point (1) is about 0·5V positive. On the negative half-cycle of the sinewave, Tr1 will be switched into conduction, but the diode action of the junction in series with the 10k Ω input resistor R2 will also clip this part of the wave. Because the sinewave is being clipped in each direction, the capacitor C1 does not charge to a steady voltage.

The waveform at (2) consists of positive-going pulses starting from supply voltage (−6V nominal) and of nearly 6V amplitude. These pulses, applied to the base of Tr2 through C2, overdrive Tr2 so that the base is cut off by the
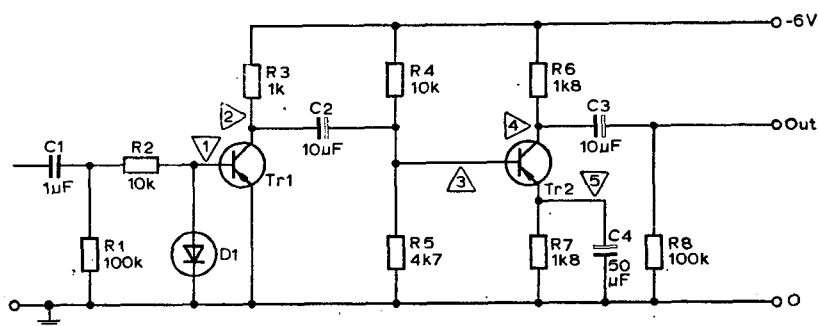
positive-going part of the pulse from C2, and the collector is bottomed by the negative-going part. In this way, the waveform from the collector of Tr2 has steep sides and a flat top; a well-shaped squarewave.

VII/1   Table of Voltage Readings

No.	1	2	3	4	5
1	0	−2·1	−2·1	−1·5	−1·6
2	0	−6·0	−1·9	−3·0	−1·3
3	−0·3	−0·3	−1·9	−3·0	−1·3
4	0	−6·0	−1·9	−3·1	−3·1
5	0	−6·0	*	−6·0	0

*indicates a very low reading

VII/2 liquid level control circuit

A typical industrial application of electronic control is the liquid level control circuit illustrated here. The electrodes, E, are mounted on an insulator in the water tank at the height of the required water level. The resistance measured between the electrodes is at least 200k Ω when the water level is below the electrodes (despite condensation), but falls to about 1k Ω when the electrodes are immersed in water.

With the water level low, Tr1 is biased off because its base is at a very low voltage and its emitter is held at a voltage of about 0·6V by the current flowing through the diode D2. With Tr1 off, the base of Tr2 is held in conduction by the connection of R3,R4,R5, so that the solenoid valve V is energised. Note that the current in the solenoid valve flows through Tr2 and so through D2, keeping Tr1 switched off. In this condition, the collector of Tr2 is at a low voltage, about 1V, and a fraction of the voltage between the supply voltage
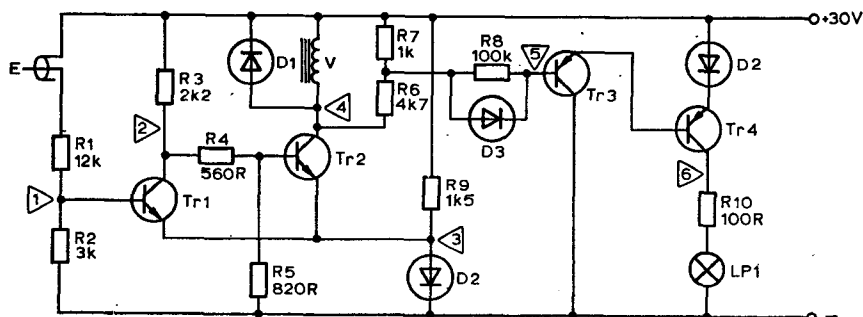
and Tr2 collector voltage is used to hold Tr3 in conduction through R8. Tr3 draws its collector current through the base of Tr4, so that Tr4 is on, and the lamp LP1 in its collector circuit is illuminated.

When the water level reaches the electrodes, E, the voltage at the base of Tr1 rises, switching Tr1 on. The voltage at point (2) drops, turning Tr2 off, so that the solenoid valve closes. The switchoff is made more rapid by the small amount of positive feedback across D2. The collector of Tr2 rises to line voltage, and C1 discharges rapidly through D3. With no bias voltage on the base of Tr3, the lamp LP1 is now extinguished.

VII/2   Table of Voltage Readings

No.	1	2	3	4	5*	6
1	0.4	5·4	0·7	1·2	24	0
2	0·4	5·4	0·7	1·2	28	27
3	0·4	1·9	0·7	28	28·5	0
4	0·4	6·8	6·3	29·8	29·8	0
5	0·4	6·8	0·7	30	30	0

*indicates that readings on this column have been taken using a FET voltmeter.

VII/3 speed stabilising circuit

Motor speed control is a very important use of electronics in industrial processes and instruments. This circuit is of a typical speed stabilising circuit for a small permanent-magnet d.c. motor, such as might be used in chart recorders or process controllers.

The motor is coupled to a small generator on the same shaft (called a tacho-generator) and this forms part of a feedback loop, since the output voltage and frequency of the pulses from the tacho-generator will be proportional to the speed of the motor. The positive-going pulses from the tacho-generator are applied through diode D1 to the potential divider formed by R1 and the circuit R2,R3,VR1,Th1, so that a fraction of the output of the tacho-generator is applied to the base of Tr1.

The diode D1 ensures that no negative pulses are applied, and also ensures that control does not start until the output of the generator is high enough to pass current through D1. The thermistor compensates for the effect of temperature changes on the base-emitter voltage of Tr1, and VR1 is used to set the running speed of the motor. The voltage measured at the base of Tr1 will always seem low, because of the pulsed nature of the waveform here.

When Tr1 conducts, the voltage level at its collector will drop, and the average collector voltage is smoothed by the large-value capacitor C1. The voltage across C1 cannot exceed the voltage set by the diodes D2–D4 and is applied to the base of Tr2. This transistor in turn controls the current in the power transistor Tr3 which is used to supply the motor.

At low motor speeds, there is no voltage on the base of Tr1, so that the base of Tr2 is high, and Tr3 conducts heavily. As the motor approaches working speed, the voltage across C1 falls, reducing the bias on Tr2 and so reducing the current flowing in Tr3. Any change of speed once the correct operating speed has been reached will cause a change in the bias on Tr1, and the correction will be fed through Tr2, and Tr3 to the motor.

In the table, one set of readings is taken under normal running conditions. The remaining readings represent fault conditions in which the motor has not stabilised at its correct running speed.
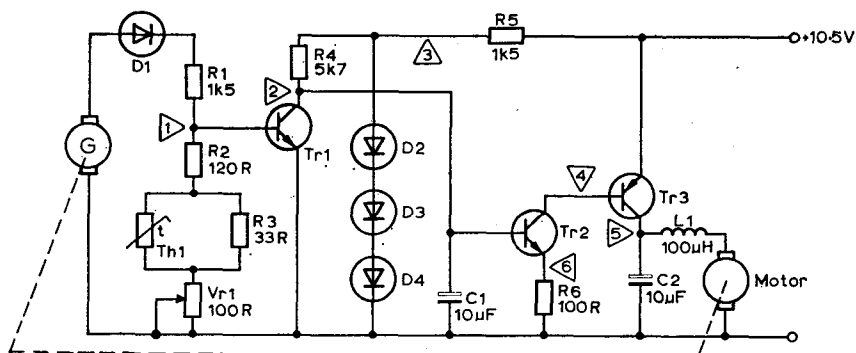

VII/3   Table of Voltage Readings

No.	1	2	3	4	5	6
1	0	1·9	2·4	9·8	9·8	1·3
2	0·2	1·7	2·4	9·9	4·1	1·1
3	0·2	0	2·4	10·5	0	0
4	0·2	0·65	2·5	10·5	0	*
5	0·2	0·5	1·6	10·5	*	0
6	0·2	0·65	2·4	9·9	4·2	*

*indicates a very low reading.
The readings in column (1) and (4) have been taken using a FET meter.

VII/4 speed stabiliser for large motor

Electronic speed control is also used for larger motors, and for other types of load. The circuit shown here is of a speed stabiliser for a larger type of motor working from a.c. mains and used to drive a machine. The motor is controlled by a triac, which switches on when triggered by a pulse (of either polarity) and switches off when the a.c. waveform crosses zero. The motor drives a small tacho-generator, G, whose output is connected in the polarity shown between the resistor chain R1,R2,R3 and the diode D1.
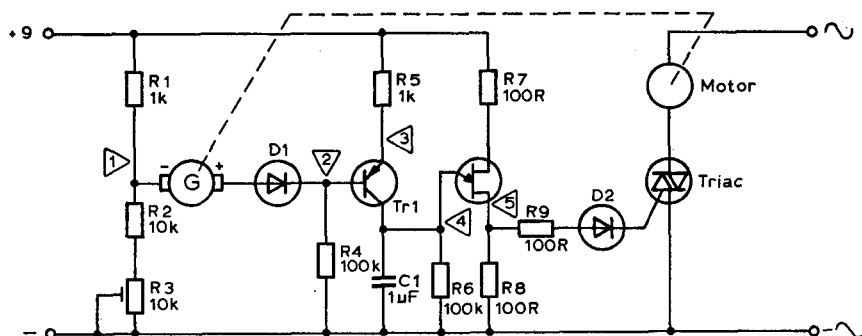
With no output from the tacho-generator, Tr1 is saturated because of the return of its base to the negative line through R4 (note that Tr1 is a p-n-p transistor), and C1 is charged rapidly through Tr1. C1 is also discharged by the unijunction, Tr2, whose output will be a series of pulses which fire the triac into almost continuous conduction.

When the tacho-generator operates, its pulse output through D1 acts to reduce the current in Tr1, so that the charging rate of C1 is much lower. This in turn means that the unijunction fires less often, so that the triac is triggered less often, and the average power into the motor is less. Note that the firing of the triac in this particular circuit is not synchronised to the mains frequency, so that the power developed on two adjacent cycles may be quite different; we rely on the inertia of the motor to average out the differences. If the supply to the controller is a full-wave rectified supply with no smoothing, the firing of the triac will be synchronised.

The voltage readings are taken at the points shown, and one set is normal; the others correspond to fault conditions. One set of oscillograms is also normal: the other represents a fault which could not readily be found by voltage readings alone.

VII/4 Table of Voltage Readings

| No.	1	2	3	4	5
1	8·6	8·45	9·0	8·6	0
2	8·6	4·6	5·2	0	0
3	8·6	8·4	Osc.	Osc.	Osc.
4	8·6	9·0	9·0	0	0
5	8·6	8·6	9·0	0	0
6	6·0	8·4	Osc.	Osc.	Osc.

NOTE: 'Osc.' means that a waveform exists at this point.
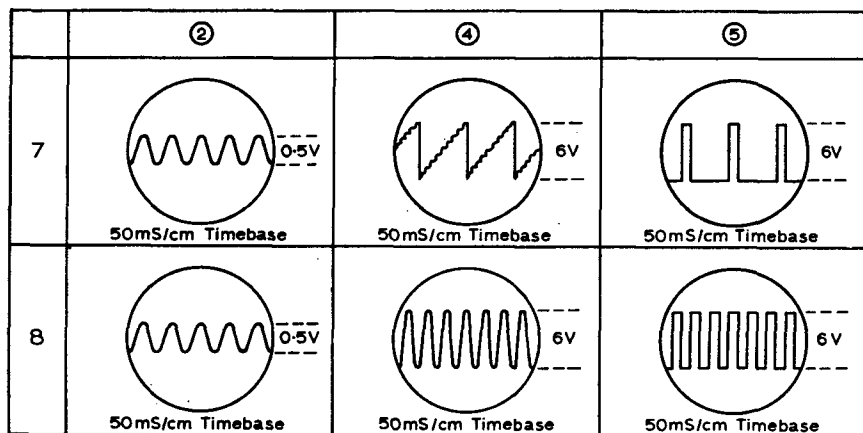
VII/5 control circuit using a relay
switched by a.c. signal

In many control circuits, a relay or solenoid, normally d.c. operated, has to be switched on or off by a small a.c. signal, often at high frequency. One example might be a safety circuit in which a door was held locked while a radio frequency oscillator was working.

In the circuit shown, the incoming frequency is applied to the base circuit of a transistor Tr1 which is biased so that it is just cut off. The positive-going parts of the waveform will switch the transistor on, causing a drop in the voltage at the collector, and the negative going peaks at the junction of the resistors R2 and R3 are smoothed by the capacitor C2, and applied to the
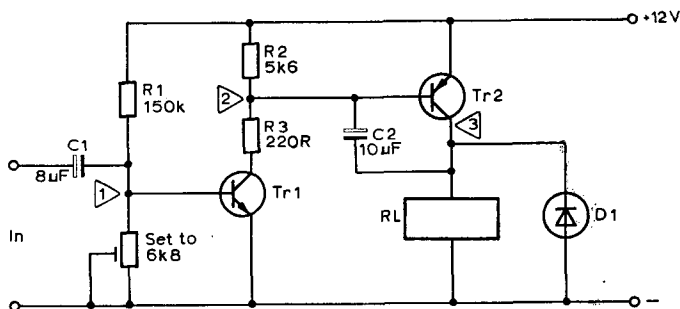
base of Tr2, a p-n-p type. The resistor R3 ensures that the voltage applied to the base of Tr2 is not so low as to cause excessive current to flow in the base circuit, possibly causing a base-emitter short. When Tr2 is switched on, the current in the collector circuit flows through the solenoid or relay coils to switch it on.

With no a.c. input, C2 charges quickly through R2, shutting Tr2 off. The relay is released, and the back-e.m.f. which is generated when the current is shut off is shorted out by the diode D1, so protecting the collector-base junction of Tr2 from damage.

The table of values is taken with no a.c. input, and one set of values is normal. The oscillograms are taken with a 300mV peak-to-peak input with a 5mS wavetime; again one set is normal. The other two oscillograms represent fault conditions, one of which could be discovered by d.c. measurements also.

## VII/5   Table of Voltage Readings

The readings at point (1) are taken using a FET voltmeter.

No.	1	2	3
1	0·5	11·8	*
2	0·5	11·4	11·4
3	0·6	11·4	11·3
4	0·5	12·0	0
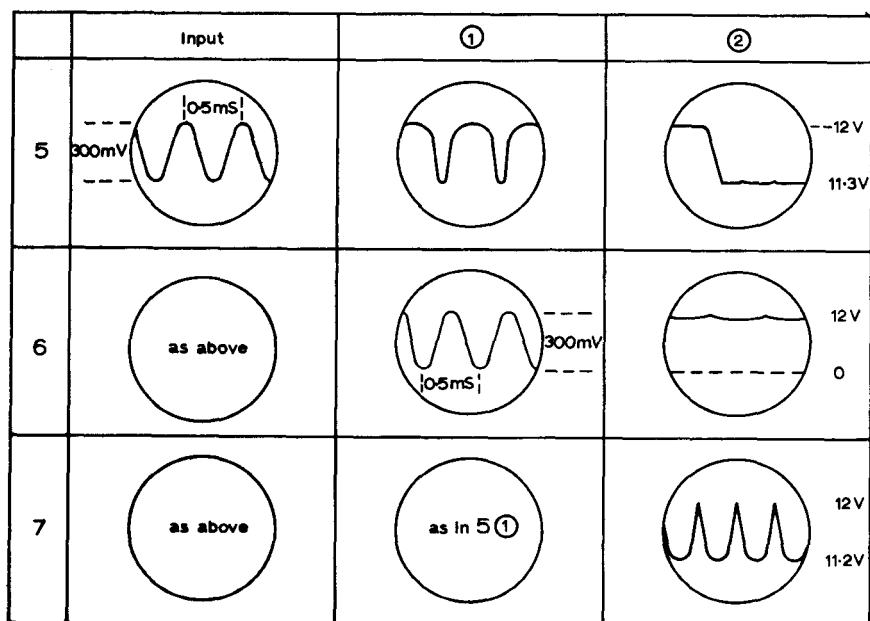
VII/6 chopper circuit
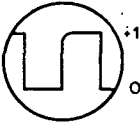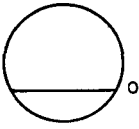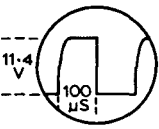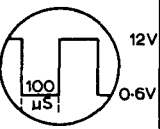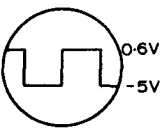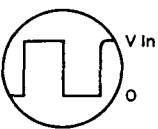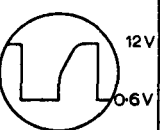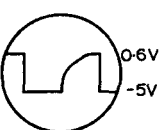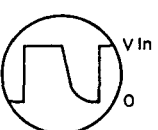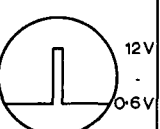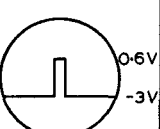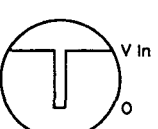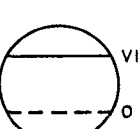
Many measuring instruments have an output which is a small change in a d.c. level, but d.c. amplification cannot easily be used for industrial applications because of the difficulty of ensuring stability. The conversion of d.c. levels to squarewaves in a 'chopper' circuit is one solution to this problem, and this circuit is an example of such a chopper circuit.
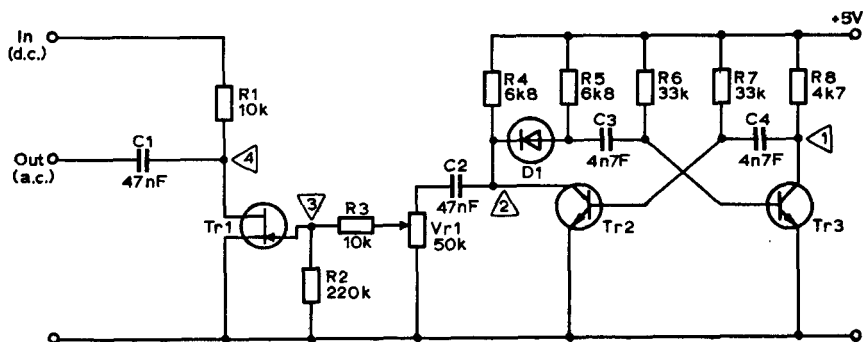
Transistors Tr2 and Tr3 are connected as a multivibrator, giving a steep-sided squarewave at the collector of Tr2. The squarewave output from the multivibrator is fed to the gate of the n-channel FET Tr1 by the attenuator VR1, and R3,R2, so that the FET is driven alternately into conduction and insulation. In the off condition of the FET, the drain is at the same potential as the d.c. input voltage; in the on condition, with the FET resistance around 100Ω, the voltage at the drain is almost zero.

In this way, the d.c. level is converted to a squarewave whose peak-to-peak value is almost equal to the original voltage. This squarewave can then be amplified in an a.c. amplifier of conventional design, and the d.c. level recovered by rectification and smoothing.

Since this is an oscillating and switching circuit, the average steady voltage readings are of no interest, and only oscillograms are shown.

	①	②	③	④
1	as in 2	as in 2	+1 / 0	0
2	11·4 V / 100 µS	12V / 0·6V / 100 µS	0·6V / -5V	V in / 0
3	as in 2	12V / 0·6V	0·6V / -5V	V in / 0
4	11·4 V / 200 µS	12V / 0·6V	0·6V / -3V	V in / 0
5	as in 2	as in 2	as in 2	V in / 0

VII/7 interface circuit to feed information into and out of digital circuits

Many industrial circuits use digital control methods, and interface circuits are needed to feed information into or out of the digital circuits. In this simplified example, changes of voltage at the input are used to drive a logic gate, and an output from the same gate is shown. In practice, of course, the input would be to one gate, and the output from another gate driven by the logic circuits.

The input to a gate using TTL is to the emitter of an integrated transistor which passes a current of 1·6mA when connected to earth (negative) for a 0 input. For a 1 input, with the input terminal connected to +4·5 to 5·25V, no current flows. In this case, the signals come from a photocell which cannot pass 1·6mA, and the input circuit is designed to amplify the current of the input signal. Tr1 is a voltage amplifier with a high voltage gain, driving the base of Tr2 which in turn drives Tr3. A + input to the base of Tr1 will cause the collector voltage of Tr1 to drop, switching on Tr2 and Tr3 and, so connecting one input of gate IC1 to the negative line.
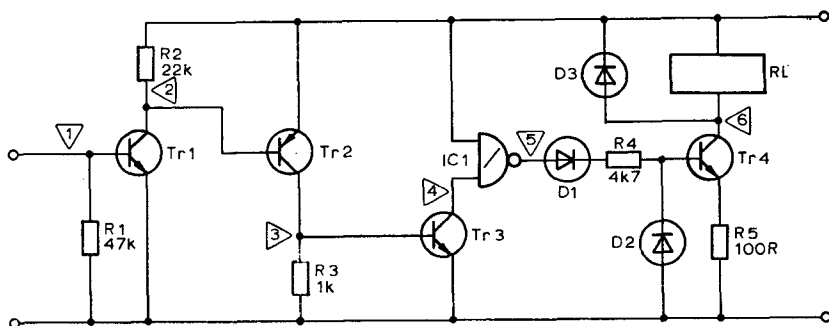
When the input to the base of Tr1 is negative, Tr3 is switched off, so that the input of gate IC1 which is connected to the collector of Tr3 is allowed to rise in voltage. With both inputs of a NAND gate high, the output voltage is low, so that the output to the base of Tr4 is zero, and no current flows in the relay. With a positive input to Tr1, making one of the gate inputs low, the output voltage of the gate is high, and Tr4 conducts, turning on the relay. The NAND gate IC1 is shown as a Schmit gate, so that the change in voltage

at the output of the gate will be very rapid (50nS or less) even if the change at the input is fairly slow. This type of gate is very often used as an interface at the input to a logic system to avoid false information being fed in by noise on slow-changing waveforms.

At the output, diode D1 and resistor R5 are used to prevent excessive base current in Tr4 when the output of IC1 goes high.

The table of readings has been taken for both input voltages, with Tr1 off (LOW) and on (0·6V on the base of Tr1).

VII/7 Table of Voltage Readings

The readings at point (2) have been taken using a FET meter. Two sets of readings have been taken in each case.

No.	1	2	3	4	5	6
1	0·6	0·6	0	4·9	0·6	12·0
	0	5·0	0	4·9	0·6	12·0
2	0·6	4·3	0·7	0·6	4·9	12·0
	0	5·0	0	4·9	0·6	12·0
3	0·6	4·3	0·7	4·9	0·6	12·0
	0	5·0	0	4·9	0·6	12·0
4	0·6	4·3	0·7	0·6	4·9	0·6
	0	5·0	0	4·9	0·6	12·0
5	0·6	4·3	0·7	0·6	0·7	0·7
	0	5·0	0	4·9	0·6	0·6
6	0·6	4·3	0·7	0·6	4·9	8·9
	0	5·0	0	4·9	0·6	12·0

VII/8 shaft rotation counter using magnetic pickup head

One frequently used method of detecting and counting shaft rotation is the use of a magnetic pickup head. This circuit shows such a head, similar in construction to the replay head of a tape recorder, connected in a circuit to interface with a digital counter. Each revolution of the shaft sweeps a magnetised part of the shaft past the head, and so inducing a voltage pulse in the

windings. The connections are chosen so that the positive-going pulse drives the positive input of an operational amplifier, so that the output of the operational amplifier will be a positive pulse of greater amplitude and power. The d.c. conditions of the operational amplifier are fixed by the return of the feedback resistor R4 to the input resistors R1 and R3, so setting the bias to 6V on both inputs.

When a small pulse picked up on the magnetic head switches the operational amplifier on, the output voltage rises to near the positive line voltage, so that ZD1 conducts, switching on Tr1. When Tr1 was off, both inputs of the Schmitt gate IC2, were high, so that the output was low (a NAND gate). When Tr1 is switched on, the gate input connected to it is shorted to negative line, and the gate output goes high. The transition of the gate output from low to high and back registers as one count into the counter circuits. Once again, the gate used is a Schmitt type so as to make the pulses fed into the counter circuits very fast rising and falling, so avoiding noise errors.

In the table of readings, the shaft has been stationary, so that there is no a.c. input.
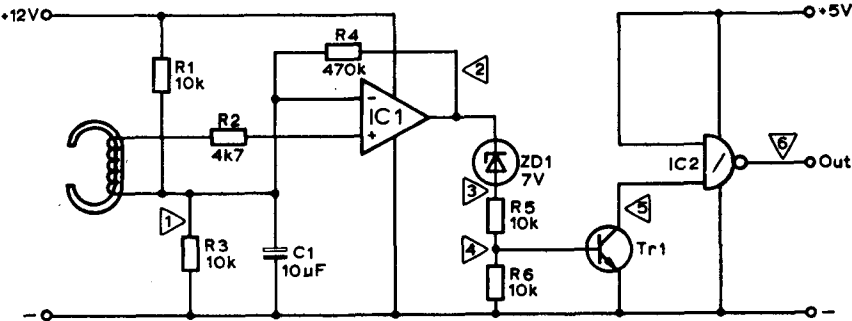
VII/8   Table of Voltage Readings

No.	1	2	3	4	5	6
1	0	12·0	5·0	0·7	0·7	5·0
2	6·0	6·0	6·0	0·7	0·7	5·0
3	11·0	0·2	0	0	4·9	0·2
4	6·0	6·0	0	0	4·9	0·2
5	6·0	6·0	0	0	0	5·0
6	6·0	12·0	5·0	0·7	0·7	5·0

DIGITAL & COUNTING CIRCUITS

VIII/1 divide-by-ten circuit

ONE OF the most important types of counting circuit used in digital instruments is the divide-by-ten circuit in its integrated form. We seldom want or need to enquire how an integrated circuit is designed, but some knowledge of the block diagram of an IC is often a useful guide to how it works and the effect of faults in the wiring or in the IC itself. The IC shown here contains four flip-flops (bistables) which would normally count to the number $2^4 - 1$
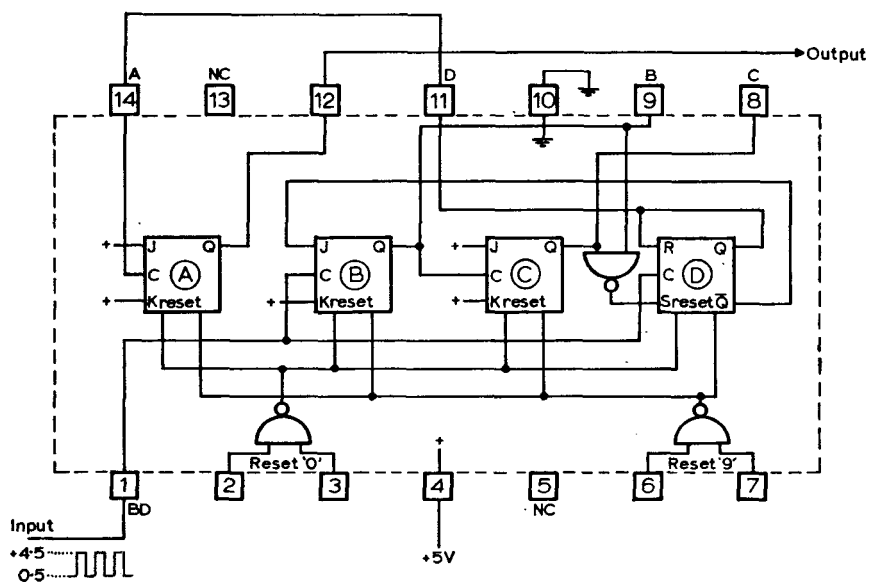
(1)					(2)			
Count	A	B	C	D	Count	A	B	C	D
0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	1	0	1	0	0
2	0	0	1	0	2	0	0	1	0
3	0	1	1	0	3	0	1	1	0
4	0	0	0	0	4	0	0	0	1
5	0	1	0	0	5	1	0	0	0
6	0	0	1	0	6	1	1	0	0
7	0	1	1	0	7	1	0	1	0
8	0	0	0	0	8	1	1	1	0
9	0	1	0	0	9	1	0	0	1

(3)					(4)			
Count	A	B	C	D	Count	A	B	C	D
0	0	0	0	0	0	0	1	0	0
1	0	1	0	0	1	0	1	0	0
2	0	0	1	0	2	0	1	0	0
3	0	1	1	0	3	0	1	0	0
4	0	0	0	1	4	0	1	0	0
5	0	0	0	0	5	0	1	0	0
6	0	1	0	0	6	0	1	0	0
7	0	0	1	0	7	0	1	0	0
8	0	1	1	0	8	0	1	0	0
9	0	0	0	1	9	0	1	0	0

(5)					(6)			
Count	A	B	C	D	Count	A	B	C	D
0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	1	0	0	0	0
2	0	0	0	0	2	0	0	0	0
3	0	1	0	0	3	0	0	0	0
4	0	0	0	0	4	0	0	0	0
5	0	1	0	0	5	0	0	0	0
6	0	0	0	0	6	0	0	0	0
7	0	1	0	0	7	0	0	0	0
8	0	0	0	0	8	0	0	0	0
9	0	1	0	0	9	0	0	0	0

(=15) before resetting. The arrangements of inputs and outputs in this IC make it possible to use the IC as a divide-by-two, a divide-by-five, a BCD counter (see later) or as a divide-by-ten as shown here.

The input, of pulses whose lower level is 0·5V or less and higher level 4·5 to 5·0V, is applied to pin 1, which is labelled as the BD input, and is applied as a clock pulse to flip-flops B and D. The pulses need not be at regular intervals. The first complete pulse will cause the Q-output of B to change from level 0 to level 1 (from less than 0·5V to about 5·0V), assuming that the counter has been reset and starts with all outputs at zero. The second pulse in will then change the B output back from 1 to 0, and the third pulse will change QB back to 1 again. The output of B is coupled to C, however, and the second pulse into B has caused the C output to change from 0 to 1. After the third pulse, the output at QB is 1 and the output at QC is 1 also. The fourth pulse changes both back to 0, and a 1 output appears at QD, which has been unable to change previously because its input to the S terminal, which is gated by the B and C outputs, has been at 0.

The 1 output at QD appears at pin 11 which is externally connected to pin 14, the input to flip-flop A. When QD has a 1 output, $\overline{QD}$ is at 0, and holds off flip-flop B by keeping the J-input low. In this way, the next pulse in turns off D (since the S input is zero) and in turn A switches on. The sixth clock pulse then clocks B from 0 to 1, and the count then continues as before with A held at 1. Just before the tenth clock pulse, the A output is 1, and D output is 1, so that B is held off again. In this way, the tenth pulse affects only the D input, whose S input is low, so that QD switches from 1 to 0, and this in turn switches QA back to zero. Since B and C outputs are already at 0, the counter is now reset. In the whole cycle of ten pulses in, the output of A goes from 0 to 1 and back, so that there is one complete pulse from pin 12 for each ten in at pin 1.

The working of logic circuits is best illustrated by truth tables which show the state (0 or 1) of each output after each input pulse. The truth tables shown here all start with the counter cleared, and show the effect of the first nine pulses in. One truth table is normal. The other faults are: one flip-flop failed (three examples); an o/s connection (one example), and a pin mistakenly returned to +5 instead of to the negative rail (one example). You are required to identify which faults have caused which of the truth table readings shown.
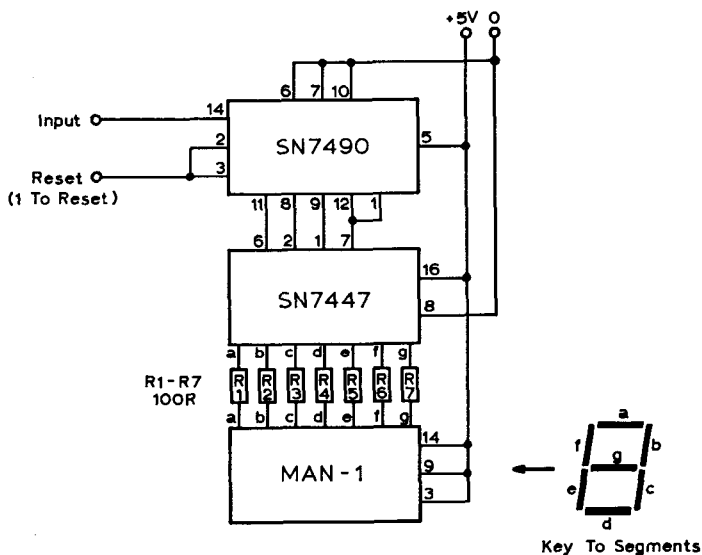
VIII/1   Truth Tables

The figure under the heading 'count' indicates the number of pulses in, the figures under the letters indicate the state (1 or 0) of each output.

VIII/2 digital display circuit

Digital voltmeters and frequency meters, calculators and counters all use the same types of digital display, the seven-segment type, which has almost superceded the earlier types. The diagram here shows the interconnections of the integrated circuits used for the display of one digit, the others being similarly arranged. Note that, as is usual for these diagrams, the pins of the ICs are not shown in the order of their actual arrangement.

The input is to pin 14 of a SN7490 counter, which gives a BCD (Binary Coded Decimal) count output on pins 8,9,11, and 12. In this form of coding, each pulse in at pin 14 changes over the state of flip-flop A, whose output is at pin 12 (A) so that a binary count (0–1–0–1–0–1–0–1 . . . .) is obtained at pin 12. The next flip-flop (B) is clocked by the output A, so that its count is 0–0–1–1–0–0–1–1– . . . . ., and C is in turn clocked by the output of B. Flip-flop D, which registers a 1 at its output only for the 8th and 9th pulse in at the input, is clocked by the output of flip-flop C, and the internal gates are arranged so that the count returns to zero on the tenth pulse in at pin 14. In the diagram, only the essential pins have been shown, and the truth table shows the outputs at A,B,C, and D for each number of the count.

The next IC is a BCD seven segment decoder, which uses the outputs from the A,B,C,D, lines of the counter to give voltages on seven output lines suitable for connecting to a seven-segment display. The lettering of the segments is shown on the diagram, and each segment is lit on this example when the voltage level on the input pin is zero. This is because this particular display uses a *common anode* connection for the light-emitting diodes; other types of

Key To Segments

display may use a common cathode display so that the segments illuminate for a 1 output.

The truth table shows the voltage levels which are present on the a,b,c,d,e,f, g, outputs of the decoder (SN7447) for each stage of the count. The connections between the decoder and the display are made through 100Ω resistors to limit the amount of current flowing in the display to prevent excessive dissipation. In this example, continuous illumination is used, but in battery operated equipment it would be more usual to 'strobe' the display, turning each digit or even (with some modern decoders) each segment on in turn for a few microseconds so as to conserve current.

The truth table shown is for the normal operation of the counter. Of the faults shown, three are caused by short circuits between connections or PCB lines, one is caused by an open circuit, and one by a line shorted to earth. The final fault is caused by an o/c resistor.

VIII/2 Faults

NORMAL TRUTH TABLE. The 'IN' column shows the number of pulses fed in at the input of the counter stage, the remaining columns show the state (0 or 1) of each labelled pin.

IN	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	1	0	0	1	1	1	1
2	0	1	0	0	0	0	1	0	0	1	0
3	1	1	0	0	0	0	0	0	1	1	0
4	0	0	1	0	1	0	0	1	1	0	0
5	1	0	1	0	0	1	0	0	1	0	0
6	0	1	1	0	1	1	0	0	0	0	0
7	1	1	1	0	0	0	0	1	1	1	1
8	0	0	0	1	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0

Faults:
(1) Voltages are normal on the BCD decoder, but segment c is missing on the display.
(2) The figures 9 and 10 are not displayed.
(3) The displayed count runs: 0,1,2,3,0,1,2,3,8,9.
(4) The displayed count runs: 0,3,3,3,4,7,7,7,8,blank.
(5) The displayed count runs: 0,1,2,3, blank until 0 again.
(6) The displayed count runs: 0,1,6,7,6,7,6,7,8,9.
In each of the above, the number of pulses into the SN7490 counter is normal for each stage of the count.

VIII/3 analogue-to-digital converter

Wherever digital methods are used, there is usually a need to convert from analogue (continuous signal) to digital or back again. The circuit here is of a 4-bit digital-to-analogue converter, which takes a binary number of up to four digits (1111 = 15) at its inputs A,B,C,D, and whose output level is a voltage proportional to the number at the input. The voltage supply is 10V, so that the output voltage is near zero for the lowest number in (1 at A) and near 10 for the highest number in (1 at each input). This is done by means of a pair of Quad Bilateral Switch ICs and the ladder network R1–R8.

The quad bilateral switches, IC1 and IC2, are MOS devices in which the resistance between two terminals (1 and 2; 10 and 11; 3 and 4; 8 and 9) is determined by the voltage level at a third terminal for each switch (13, 12, 5, 6). At a low voltage input to the switch pin, the resistance between the other two pins is very high, but for a high voltage on the switch pin (+5V or more) the resistance is very low, so that each unit acts as a switch controlled by the voltage input, and there are four switch circuits in each IC. Since the current can pass in either direction when the switch is on, the circuit is described as bilateral.

The ladder network is an extended voltage divider, with the output (feeding into a 1MΩ load) taken from the point where the D-output feeds in. The outputs of the switches at M,N,O,P, may be at 0 or +10V according to whether the inputs at A,B,C,D are 0 or 1, and the output at V_{out} will be decided by the various combinations of voltages at M,N,O,P. The complete analysis of such a network is by no means simple, and some approximations have to be made, but the steps of voltage in this example are of the order of 0·7V, and are approximately equal.
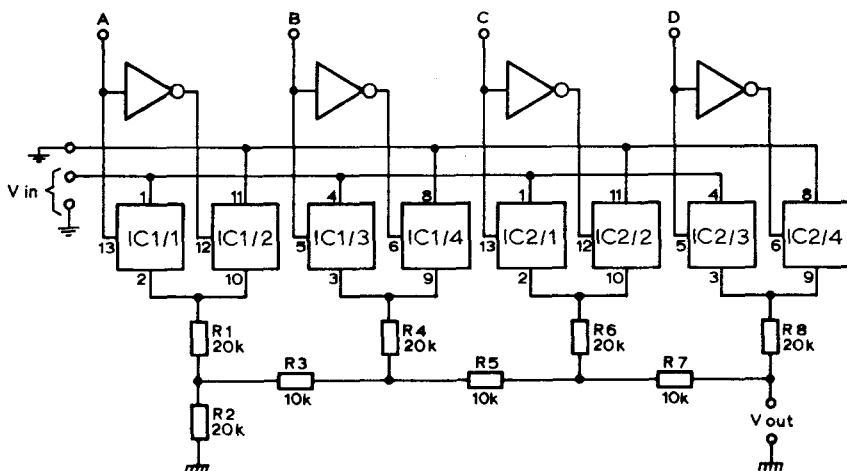
The truth table shows the voltage steps aimed at for a count of 15. From a maintenance point of view, the faults which may appear will be switch faults or resistor faults. The questions require you to identify, without attempting to analyse the circuit in detail, what resistor or switch defects could cause the faults in particular steps as shown.

VIII/3   Truth Table and List of Faults

TRUTH TABLE. The first column is of the number of pulses into the BCD counter (not shown in diagram) which feeds the converter. The remaining columns show the voltage levels at the marked points, taken using a FET volt-meter. The load on the output terminals is not less than 1M Ω.

| No.	A	B	C	D	M	N	O	P	Vout
0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	10	0	0	0	0·66
2	0	1	0	0	0	10	0	0	1·33
3	1	1	0	0	10	10	0	0	2·0
4	0	0	1	0	0	0	10	0	2·6
5	1	0	1	0	10	0	10	0	3·3
6	0	1	1	0	0	10	10	0	4·0
7	1	1	1	0	10	10	10	0	4·6
8	0	0	0	1	0	0	0	10	5·3
9	1	0	0	1	10	0	0	10	5·9
10	0	1	0	1	0	10	0	10	6·7
11	1	1	0	1	10	10	0	10	7·3
12	0	0	1	1	0	0	10	10	7·9
13	1	0	1	1	10	0	10	10	8·6
14	0	1	1	1	0	10	10	10	9·3
15	1	1	1	1	10	10	10	10	10

Faults:

(1) Steps no.'s 2,3,6,7,10,11,14,15 are low in voltage output.
(2) Steps from No.7 onwards give lower than normal output.
(3) Every ODD step (1,3,5, etc) gives higher than normal output.
   THE ABOVE FAULTS ARE RESISTOR FAULTS
(4) Each EVEN step gives a higher than normal output, and there is a reading of about 0·6V even with no pulse input.
(5) Steps 4 to 7 and 12 to 15 give lower than normal output voltage.
(6) Steps 0 to 7 give higher than normal output voltage.
   THE ABOVE FAULTS ARE SWITCH FAULTS.

VIII/4 parallel-to-serial converter

The information placed into counter circuits may be in serial or parallel form. Serial information is in the form of a train of pulses which can be taken to one input, since the pulses do not occur simultaneously. For example, the input to the counter in circuit VIII/1 is serial. Parallel information consists of voltage levels at several inputs which will occur at the same time; for example, the input to the D-A converter of circuit VIII/3 is parallel at the A,B,C,D, inputs.

In many computing circuits, these types of information have to be converted. Serial information may have to be converted to parallel form to be added to another number in parallel form; parallel information may have to be converted to serial to be divided in a counter circuit, and so on.
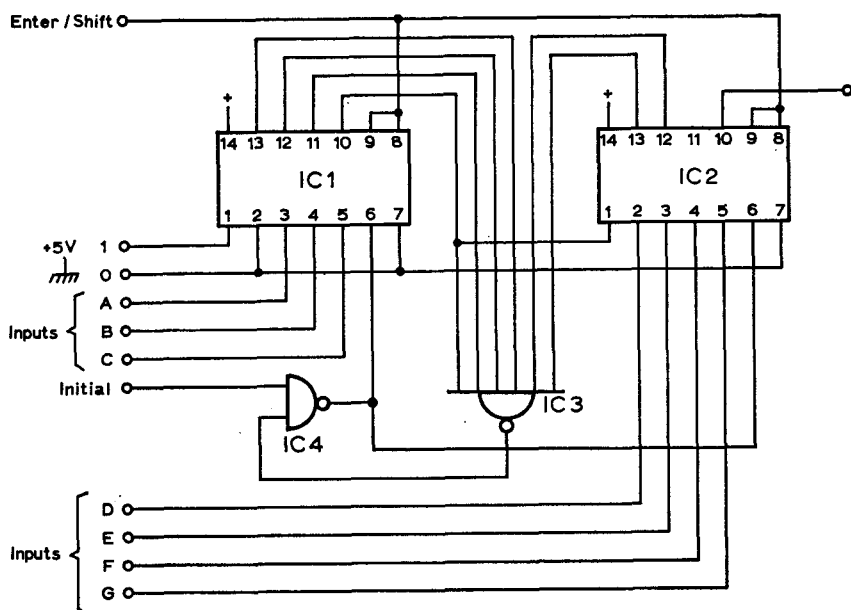
The diagram here shows a seven-bit (up to $1111111 = 127$) parallel-to-serial converter using the SN7495 shift register ICs. Shift registers are arrangements of flip-flops whose outputs can be set to 1 or 0 by preset inputs. Each clock pulse in can be arranged to shift the number (0 or 1) stored in each flip-flop to the next flip-flop in line, either to the right or to the left. The shift register ICs shown here have the additional facility of a 'mode control input' at pin 6.

When pin 6 is returned to 0, each clock pulse will shift information from the input flip-flop to the next in line and so on to the output (right shift).

In this way, information which is at pin 1 on one clock pulse will be shifted to the next flip-flop on each clock pulse and will come out of the register a definite number of clock pulses later. In addition, voltages at the parallel inputs (presets) on pins 2,3,4,5 are gated out so that they have no effect on the register. With a 1 input at pin 6, however, the information at pins 2,3,4,5, is entered into the register, and the clock pulses cause no shifting.

In the circuit shown, the voltage at pin 6 of each of the registers is normally low, because the NAND gate IC4 has one high input from IC3 and one high input at the INITIAL input. In this state, the register will shift at each clock pulse, but no information has been entered. When a negative pulse (1 to 0) is applied at the INITIAL input, the output of IC4 goes high, so that pin 6 on each register is high, and the information at pins 2,3,4,5 on each register will enter at the next clock pulse. Since pin 2 is returned to earth, the first flip-flop stores a 0, and the remainder store the seven-bit number which was present on the inputs.

At the end of the INITIAL pulse, which does not have to be repeated, pin 6 voltage returns to 0. Each clock pulse will now shift the information one step on in the register, and the input on pin 1 is gated to the first flip-flop. Since this pin is returned to the + line (1), a 1 will be entered at each clock pulse.

After seven clock pulses, all the registers have a 1 stored except the last two, which have a 0, and the last number entry which appears at pin 10 of IC2, the last of the pulses to appear at that pin in serial form. The six inputs to the gate IC3 are now all 1, so that the output is 0, causing IC4 to give a 1 output, and activating another entry of data at the parallel inputs without any need for an INITIAL pulse. Note that any change in the voltages at the parallel inputs while the register is shifting makes no difference to the serial number read out, since these inputs are gated out while the voltage on pin 6 is low.

Four possible faults are given, each of which might be caused by a connection failure (o/c or s/c)

VIII/4   Faults List

(1) One cycle of conversion proceeds normally, but the cycle does not repeat unless the INITIAL switch is used again.
(2) The INITIAL pulse has no effect, but the registers appear to be working normally.
(3) Inputs D,E,F,G, shift out of the register, but inputs A,B,C, do not appear at the output.
(4) No pulses appear at the output. D.C. supplies are normal.

VIII/5 serial-to-parallel converter

The opposite conversion of serial to parallel can also be carried out by a pair of SN7495 shift registers, along with a NOR gate and inverter. Once again, the 'mode control' pin 6 is used in each register to control the action of the register; the voltage at pin 6 is normally low.

A positive pulse at INITIAL causes the output of the NOR gate to go low, and the output of the inverter to go high, raising the voltage at pin 6 on each register and allowing parallel entry on pins 2,3,4,5 in each register at the next clock pulse on the ENTER line. Since pin 3 of IC1 is connected to the + line (1), and the remaining pins 4 and 5 on IC1 and all the entry pins on IC2 are earthed (0), the number which is entered on this first ENTER pulse is the first serial number (0 or 1) at the input (pins 1 and 2) along with a 1 at pin 3 and zeros in all the other registers. We can write this entry as D1000000, where D is the voltage level (0 or 1) at the serial input.
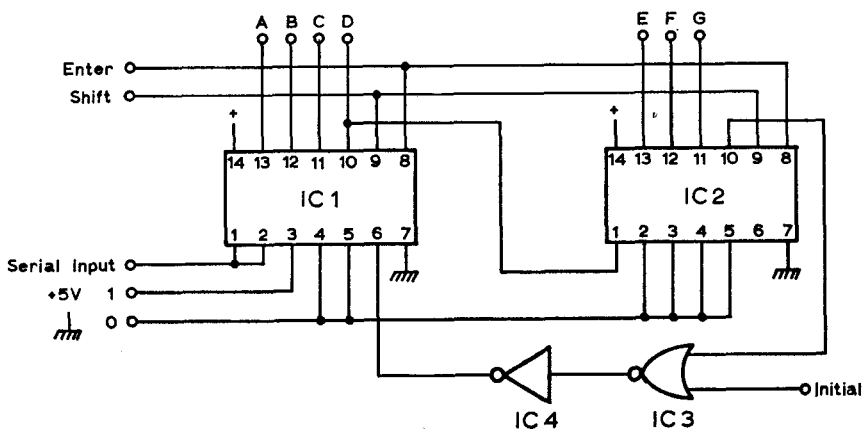
When the voltage at pin 6 returns to 0 at the end of the initial pulse, clock pulses on the SHIFT line will cause the stored numbers to shift to the right and the serial information will enter at pin 1 on IC1. Since each flip-flop in the register after the first two of IC1 was set to zero at the beginning of the cycle, each shift pulse will give a zero output at pin 10 of IC2 until seven shifts have taken place. At this time, the outputs on the register output pins 13,12,11,10

on IC1 and 13,12,11 on IC2 consist of the voltages present at the serial input at each clock pulse.

When the next SHIFT pulse occurs, a 1 appears at pin 10 of IC2 and operates the NOR gate (this is the 1 which was loaded in at the beginning of the cycle) starting off the cycle again with no need for an INITIAL pulse. The ENTER line is active only when pin 6 of each IC is at 1, and the SHIFT line is active only when pin 6 is at 0, so the same clock pulses can be used with no additional gating.

The fault symptoms shown are caused by o/c connections which should be readily identifiable from this description of the action of the circuit.

VIII/5   Faults List

(1) No data appears at the outputs. D.C. supplies are normal, and the gates are working.
(2) The INITIAL pulse has no effect.
(3) The cycle does not repeat.
(4) Only the first four bits appear at the outputs A,B,C,D.

VIII/6 Johnson counter

The final diagram is of a Johnson counter, which uses a different type of coding as compared to the binary counters in the other circuits in this section. A Johnson counter is easy to design, and the outputs are easily decoded to give a decimal output; in addition, the type of coding makes faults easy to detect.
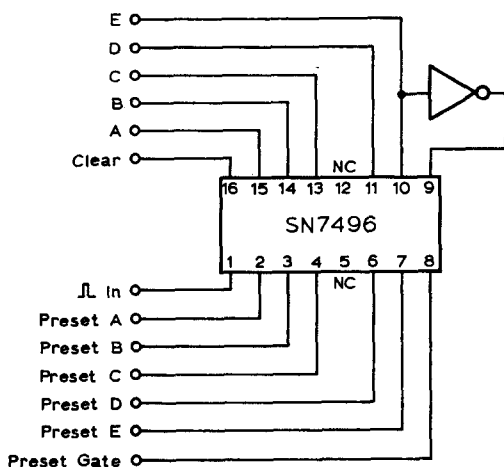
The integrated form of a Johnson counter shown here uses a SN7496 shift register with the external connections shown. The 7496 is a 5-bit register containing five flip-flops with gated outputs. The only interconnection needed to convert this into a 10-step Johnson counter is the connection of the E output on pin 10 to pin 9, through an inverter. With a positive-going pulse in put at pin 1, the counter then gives outputs on pins 15,14,13,11, and 10, labelled A,B,C,D,E.

The truth table is shown in the diagram, and the coding is self explanatory. The decoding is also shown, and we can see that only two gate inputs are needed for decoding any number. The bar symbol means 'inverse', so that $\bar{A}\bar{E}$ means that a gate should give a 1 output when both A and E are low, this

occurs only for the decimal zero. Similarly $C\bar{D}$ means an output when C is at 1 and D at 0, which occurs only when the count is 3.

The questions relate to various false outputs which may be due to unwanted inputs, shorts between lines on the PCB or to earth, or to a misconnection between pins 9 and 10

VIII/6 Truth Table and Faults List

TRUTH TABLE. The column labelled DEC. is the decimal count, the number of pulses in to the counter. The lettered columns show the state (1 or 0) of each output of the counter.

DEC	A	B	C	D	E	DECODE	
0	0	0	0	0	0	$\bar{A}$	$\bar{E}$
1	1	0	0	0	0	A	$\bar{B}$
2	1	1	0	0	0	B	$\bar{C}$
3	1	1	1	0	0	C	$\bar{D}$
4	1	1	1	1	0	D	$\bar{E}$
5	1	1	1	1	1	A	E
6	0	1	1	1	1	$\bar{A}$	B
7	0	0	1	1	1	$\bar{B}$	C
8	0	0	0	1	1	$\bar{C}$	D
9	0	0	0	0	1	$\bar{D}$	E

FAULTS. What faults might be suspected in the following cases?
(1) The counter output is 11011.
(2) All outputs are zero, d.c. supply is normal, pulses in normal.
(3) The counter does not return to zero after a count of 9.
(4) The figures 4 and 9 appear together at the display.

GENERAL NOTES
ON COMPONENT FAILURE

Resistors

These generally fail by going open-circuit or increasing to a much higher resistance value. Wire-wound resistors fail in this way due to electrolytic corrosion in acid or simply moist atmospheres. Cracked-carbon and metal film resistors are damaged readily by over-dissipation, particularly when placed near to high-wattage wire-wound types.

Capacitors

Failure of the small value types is uncommon, but plastics dielectric types in the 10nF to 1μF range sometimes go open-circuit. Electrolytics are much less reliable, often going short circuit, sometimes open. High a.c. currents will cause rapid failure of electrolytics, unless the capacitor has been specifically designed for such use (as a reservoir capacitor in a power pack, for example). High operating temperatures are also a factor leading to short life.

Inductors

These are generally the most reliable of components, but can suffer from electrolytic corrosion, going open circuit. Though rare on mains transformers, pulse transformers can sometimes suffer from shorted turns which causes a great deterioration in the pulse performance but is impossible to check by resistance readings.

Diodes

Like other semiconductors, diodes are easily damaged by short overloads of current or voltage. They may go open-circuit, rather more rarely short circuit. The ratings of diodes must be carefully checked, since reverse voltage or current ratings can often be exceeded when a short pulse occurs on a supply line.

Transistors

Generally reliable, but easily damaged as the result of failure of other components. The most common failure is s/c emitter to base, with o/c collector junction, but high leakage from emitter to collector is also found. Damage can be due to momentary over-dissipation, particularly when the transistor is running near its limits at high temperatures.

Integrated Circuits and other Semiconductors

Again generally reliable, and usually found in circuits where they are protected from the damaging results of unwanted pulses. Thyristors and other semiconductors also have reasonably good reliability records, but thyristors can fail in a way which can cause considerable damage, when the gate control action ceases, with the gate s/c.

ANSWERS

In this section, the component failures which caused the original readings are identified, along with the normal set of readings. In some cases, more than one component can cause the fault, and it is a good exercise to discuss what additional tests might be carried out, before removing any components, in order to identify the faulty component more closely. Where the failure is not completely obvious from the readings, the tell-tale signs have been identified.

SECTION I: POWER SUPPLIES

I/1 Set 2 is normal.
(1) C1 o/c, the voltages are those we would expect with no smoothing.
(3) Mains fuse blown is most likely, o/c in transformer winding less likely.
(4) Rectifier diode o/c; a.c. but no d.c.
(5) ZD1 o/c, so that there is no regulation, leading to high output (2).
(6) ZD1 s/c, therefore no regulated output.

I/2 Set 4 is normal.
(1) One diode in the bridge is o/c, so that the voltages correspond to half-wave rectification. How could you identify which diode was o/c?
(2) C1 is o/c, so that the bridge does not feed into a reservoir. The voltage measured at (2) is the full-wave unsmoothed value. The rest of the smoothing circuit now acts as a choke input filter, with reduced output voltages.
(3) Choke is o/c, an unusual fault which might be found in an old supply operated in a damp atmosphere (for example, an electroplating supply).
(5) R1 o/c, making the regulated output zero. Failure of the zener (short circuit) would also cause zero output, but the higher values of voltage in the

rest of the circuit indicate that less current is being taken.
(6) Zener diode o/c, so the output is unregulated at (4)

I/3   Set 5 is normal.
(1) R2 is s/c, so that there is no bias on Tr1
(2) R1 is o/c, so that Tr1 is conducting heavily.
(3) Tr1 has a base-emitter s/c, collector o/c.
(4) The regulator IC has failed, since the voltage between (2) and (4) is not 12V
(6) C1 is o/c, so that the supply is unsmoothed.

I/4   Set 5 is normal.
(1) R1 is o/c, so that there is no supply to the zener. Some output voltage would be measured when the circuit was switched on, but not thereafter.
(2) ZD1 is o/c, so that there is no stabilisation, and C1 charges to peak voltage.
(3) C1 is o/c, so the meter reads average unsmoothed voltages
(4) Th1 is o/c.
(6) Th1 is s/c, and there is no regulation, though zener voltage is normal..

I/5   Set 3 is normal.
(1) C3 is o/c, so that there is considerable ripple, and the full d.c. is not measured on the meter.
(2) D1 is o/c, so that only a.c. can be measured here.
(4) D2 is s/c, preventing the second multiplication step.
(5) R1 is high, causing a large voltage drop even with a small load.
(6) C2 is o/c, preventing the first stage from operating. The voltage measured is probably due to leakage.

I/6   Set 3 is normal.
(1) R5 has gone high, causing the abnormally low reading at (4)
(2) Load s/c, because the overload protection is working.
(4) R3 is o/c. The rise in supply voltage is caused by the very small current being drawn, since this can only pass through the base-emitter of Tr1.
(5) ZD1 is o/c, so that the voltage at (3) is unregulated.

I/7   Set 2 is normal.
(1) C4 is o/c, voltage values are for unsmoothed circuit.
(3) Half of the transformer winding is o/c. Since the winding will be heavy gauge, this is probably caused by a connection failure.
(4) Tr2 has failed, with base-emitter s/c and collector o/c.
(5) R1 has gone high, restricting the current swing in Tr1.
(6) One of the bridge rectifiers has failed, so that the on-load output voltage is down.

SECTION II: AUDIO FREQUENCY AMPLIFIERS

II/1   Set 2 is normal.
(1) Tr2 is faulty, base-emitter s/c, collector o/c
(3) R5 has gone high, the reduced bias causes point (2) to go high.
(4) R3 has gone high, reducing the current in Tr2.
(5) Tr1 has base-emitter s/c, collector o/c; or the 100k(R5) is o/c.
(6) C2 is o/c, causing negative feedback of signal.

II/2   Set 1 is normal.
(2) The transformer primary winding is s/c, causing high reading at (4).
(3) R3 is o/c, causing bias failure to Tr2.
(4) R6 is o/c, so that no current flows in Tr3.
(5) Tr2 is faulty, base-emitter s/c, collector o/c. R3 feeds into R4.
(6) R1 is o/c, so that there is no bias on Tr1.

II/3   Set 5 is normal.
(1) R4 is s/c, shorting the bases of Tr3,Tr4 together, so that no output current flows in these transistors.
(2) R5 has gone high, so that only voltages above R5 are normal.
(3) Tr1 failure, base-emitter s/c, collector o/c.

(4) R6 has gone high, causing all the voltage readings to be low.
(6) Tr2 o/c, so that Tr3, Tr4 are over biased

II/4 Set 3 is normal.
(1) Tr1 faulty, base-emitter s/c, collector o/c. The high collector voltage has switched the IC output to low, and the other transistor has therefore been biased off to make the voltage at the + input of the IC follow.
(2) R2 has gone high, the drop in current has caused the high voltages at the collectors.
(4) R4 has gone high, causing low collector voltage. Because of the following action of the IC, similar readings would be obtained with R3 high.
(5) The IC has failed, with a permanently high output due to an internal short.
(6) The IC has failed, with permanently low output due to an internal short.

II/5 Set 1 is normal.
(2) C2 is s/c
(3) Tr2 faulty, base-emitter s/c, collector o/c.
(4) Tr1 faulty, base-emitter s/c, collector o/c.
(5) R2 high, causing high voltage at (1).
(6) R1 o/c, so that Tr1 is unbiased.
(7) C2 is o/c, so there is no 'bootstrap' feedback.

II/6 Set 2 is normal.
(1) D1 is s/c, so that the voltage at (3) is too high.
(3) Tr2 failed, base-emitter s/c, collector o/c.
(4) R2 is o/c.
(5) Tr1 faulty, base-emitter s/c, collector o/c.
(6) Tr3 faulty, base-emitter s/c, collector o/c.

II/7 Set 5 is normal.
(1) Phototransistor is s/c, indicated by voltage at (1).
(2) R6 has gone high, reducing bias on Tr1.
(3) R8 has gone high, reducing current in Tr1.
(4) Tr1 failure, base-emitter s/c, collector o/c.

(6) C4 is s/c, so that excessive current flows in Tr1.

(7) Phototransistor is o/c, high voltage at (1)

II/8   Set 3 is normal.

(1) The IC gate is o/c.

(2) R2 has gone high, so that Tr1 cannot be switched to a high current.

(4) R4 has gone high, keeping Tr3 base voltage low.

(5) Tr2 has failed, base-emitter s/c, collector o/c.

(6) Tr1 has an o/c collector, probably caused by failure of D2

SECTION III: TIMING CIRCUITS

III/1   Sets all indicate faults.

(1) C1 is s/c, shorting out point (3).

(2) Tr2 is o/c.

(3) Tr1 failure, base-emitter s/c, collector o/c.

(4) R5 has gone high (or R6 very low).

(5) Input shorted, caused by R4 gone high.

III/2   Sets 2 and 5 are normal.

(1) Tr1 has failed, base-emitter s/c, collector o/c.

(3) IC1 has failed, output low resistance to positive supply.

(4) R4 high or o/c, so that delay is very long.

(6) R6 or D2 s/c. A transistor failure would leave some signal across R7.

(7) D2 o/c, not clipping spike.

(8) R2 low (or leaky capacitor C2), short time delay.

III/3   Sets 2 and 5 are normal.

(1) R3 high, causing almost normal voltage levels but slow charging.

(3) D1 o/c, no supply to timer.

(4) R2 gone low, keeping trigger voltage low.
(6) C3 o/c, timer operating on stray capacitance.
(7) C2 o/c, pin 2 not held low for long enough to trigger.

III/4   Sets 2 and 6 are normal.
(1) D3 is o/c, no collector voltage on Tr2.
(3) Tr1 faulty, base-emitter s/c, collector o/c, or D2 o/c, causing no bias.
(4) Tr2 faulty, base-emitter s/c, collector o/c.
(5) D1 is s/c, holding Tr1 on.
(7) R2 high, so that C4 charging time is long and switching takes place before the voltage on the collector of Tr1 has changed much. Output pulse low.
(8) R5,R6 faulty, not passing pulse to Tr2.
(9) R1 or C2 faulty, time delay is too short.
(10) D4 is s/c, passing both polarities of pulse.

III/5   Sets 2 and 8 are normal.
(1) Tr2 faulty, base-emitter s/c, collector o/c.
(3) ZD1 o/c, voltage between (3) and (4) is incorrect.
(4) Tr1 failure, collector-emitter leakage.
(5) R3 high, could also be failure of ZD1.
(6) Tr3 failure, base-emitter s/c, collector o/c.
(7) C1 o/c, no sawtooth developed.
(9) R1 or VR1 high, time of sweep much too long.

III/6   Sets 3 and 8 are normal.
(1) Zener diode ZD1 is o/c. The bias on Tr1 is low, though the output of the IC is high.
(2) R4 is o/c. Tr3 is unbiased, and Tr2 is off.
(4) Tr1 is faulty. Base-emitter s/c and collector o/c, no bias at input though IC output high, also Tr2 fully on.
(5) Zener diode ZD2 is s/c, so that IC1 cannot operate properly.
(6) Tr2 is faulty, base-emitter s/c, collector o/c. Its base is at a low voltage despite the fact that Tr1 is cut off.
(7) Tr3 faulty, base-emitter s/c, collector o/c. R4 and R5 act as a voltage divider, with no trace of transistor action.
(9) R4 has gone high, so that the time constant for flyback is greatly increased.

SECTION IV: MEASURING CIRCUITS

IV/1   Set 3 is normal.
(1) One of the diodes, D1,D2, or D3, is s/c, hence low voltages at points (1) and (2).
(2) The selector switch is o/c, or Ry o/c, making the voltage at point (4) very low.
(4) The potentiometer VR2 is wrongly set, so that there is an offset.
(5) R1 has gone high, lowering the voltages at the input.
(6) LED1 is s/c.

IV/2   Set 4 is normal.
(1) The switch contacts are o/c on this range, or IC not working.
(2) R2 has gone high.
(3) VR1 incorrectly adjusted, so that there is an offset voltage.
(5) VR2 incorrectly adjusted, so that amplifier gain is reduced.
(6) R3 is o/c, so that voltage division does not take place.

IV/3   Set 2 is normal.
(1) R9 or R10 has gone high, so that the gain is low.
(3) VR2 is incorrectly set, making the gain too low.
(4) Switch contact Sw1b is o/c, no feedback.
(5) VR1 is out of adjustment, so that there is an offset voltage.
(6) C3 is s/c or VR2 or R11 o/c.

IV/4   Set 2 is normal.
(1) R6 has gone high, so that the voltage supplied to the bridge circuit is low.
(3) VR1 has been set too low.
(4) Thermistor is o/c.
(5) VR1 has an o/c wiper contact, so that the + input to the IC is floating.
(6) R2 is o/c.

IV/5   Set 4 is normal.
(1) The ORP12 is o/c.
(2) Tr1 faulty, base-emitter s/c, collector o/c.
(3) R2 has gone high, so that Tr1 and Tr3 saturate at a very low current, insufficient to drop enough voltage across R5 and R6.
(5) Tr3 is faulty, base-emitter s/c, collector o/c.
(6) One of the diodes is s/c, altering the voltage drop.

IV/6   Set 7 is normal (oscillograms).
(1) R1 has gone high, or zener failed, so that no stabilised voltage is obtained.
(2) Tr1 faulty, base-emitter s/c, collector o/c.
(3) Switch contacts faulty, no current flowing to Tr1.
(4) Tr1 faulty, high leakage from collector to emitter.
(5) Probably R5 s/c, or high resistance in Tr1 leads.
(6) Gate has o/c input at B, oscillation normal, but no output from the buffer stage. R7 cannot be o/c, otherwise there would be no oscillation at point (7).
(8) Tr2 is not switching correctly. R6 may be s/c, or there is a high resistance connection to the transistor.

SECTION V: OSCILLATORS

V/1   Set 2 is normal.
(1) C2 is s/c, or R3 is s/c.
(3) Tr1 faulty, base-emitter s/c, collector o/c.
(4) R1 has gone high, insufficient bias.
(5) Transformer primary winding o/c, or no connection to collector.
(6) C2 probably o/c, or transistor gain very low.
(7) Overbiased, R1 low, or R2 high.
(8) C1 o/c or disconnected.

V/2   Set 4 is normal.
(1) C4 is s/c or R8 s/c.
(2) R1 has gone high, reducing bias.
(3) R5 has gone high, so that Tr2 saturates.
(5) Tr1 faulty, base-emitter s/c, collector o/c.
(6) C4 is o/c, so that gain is low.

V/3   Set 2 is normal.
(1) Tr3 faulty, base-emitter s/c, collector o/c.
(3) Tr2 faulty, base-emitter s/c, collector o/c.
(4) R4 has gone high, making the collector voltage of Tr1 very low despite normal bias.
(5) R3 has gone high, causing large difference between voltages at points (2) and (3).
(6) Tr1 faulty, open circuit.
(7) One or both diodes o/c.

V/4   Set 4 is normal (oscillogram only)
(1) Tr2 faulty, base-emitter s/c, collector o/c.
(2) Slider of VR1 is o/c, no charging or discharging taking place.
(3) Tr1 faulty, base-emitter o/c.
(5a) VR1 slider is set to the end nearest R1.
(5b) VR1 slider is set to the end nearest R2.

V/5   Set 5 (oscillograms) is normal.
(1) Tr1 faulty, base-emitter s/c, collector o/c.
(2) D1 o/c, so that Tr2 cannot affect base of Tr1.
(3) Tr2 has failed, base-emitter s/c, collector o/c.
(4) D1 is s/c, allowing long rise time at the collector of Tr2.
(6) R2 has gone high, so that the time constants are unbalanced.
(7) C3 is leaky, causing the load on Tr2 to be excessive, and the collector voltage to remain low, though oscillation continues. While oscillation continues, this fault cannot easily be deduced from d.c. measurements.

V/6   Oscillogram 7 is normal; the 'normal' voltages are indicated.

(1) C1 is s/c, no bias on Tr2.

(2) C2 is s/c, no bias on Tr1.

(3) R3 has gone high, large difference between points (3) and (5).

(5) R1 has gone high, voltage at point (1) is low.

(6) R2 has gone high, low voltage at (2).

(8) C1 is disconnected, so that oscillation continues using stray capacitance, at a high frequency.

SECTION VI: TRIGGER CIRCUITS

VI/1   Set 4 is normal.

(1) Tr1 is faulty, base-emitter s/c, collector o/c, so that base voltage is equal to emitter voltage when the 8·2k Ω resistor is earthed.

(2) R5 has gone high, so that Tr2 saturates.

(3) Tr2 is faulty, o/c, so that only Tr1 passes current.

(5) R2 has gone high, keeping Tr2 biased off.

(6) R3 is o/c, keeping Tr2 on.

VI/2   Set 2 is normal.

(1) Tr3 is faulty, base-emitter s/c, collector o/c.

(3) Tr1 is faulty, open circuit, so that bias at (1) is decided by voltage across R3 caused by current through R7,R8.

(4) Tr2 is faulty, base-emitter o/c, collector o/c, some bias due to Tr1 is present.

(5) ZD1 is o/c (or 470 Ω o/c).

(6) R6 has gone high.

VI/3   Sets 4 and 6 are normal.
(1) Tr1 faulty, base-emitter s/c, collector o/c.
(2) C1 s/c, possibly R6 o/c.
(3) SCS is o/c, or LED in opto-coupler o/c.
(5) Tr2 faulty, base-emitter s/c, collector o/c.
(7) Tr2 o/c or R6 o/c, or faults in R7,VR1, Th1.
(8) One diode o/c in power supply.

VI/4   Set 2 is normal.
(1) Tr3 faulty, base-emitter s/c, collector o/c; or Tr6 leaky.
(3) Tr9 faulty, base-emitter s/c, collector o/c.
(4) Tr7 o/c or Tr8 o/c.
(5) R3 high.
(6) Tr5 faulty, base-emitter s/c, collector o/c.

SECTION VII: CONTROL & INTERFACE CIRCUITS

VII/1   Set 2 is normal.
(1) C2 is s/c, causing excessive base voltage on Tr2.
(3) Tr1 faulty, base-collector s/c, emitter o/c.
(4) Tr2 faulty, leakage between emitter and collector.
(5) R4 has gone high, reducing bias on Tr2.
(6) C4 is s/c, saturating Tr2.

VII/2   Set 2 is normal.
(1) D4 o/c or Tr4 o/c.

(3) R3 has gone high, so that Tr1 is saturated.
(4) D2 is o/c.
(5) Tr2 has failed, o/c.

VII/3   Set 6 is normal.
(1) Tr1 has failed, base-emitter s/c, collector o/c, or D1 o/c, R1 o/c.
(2) R6 has gone high.
(3) C1 is s/c.
(4) Tr3 faulty, base-emitter s/c, collector o/c.
(5) D2,D3, or D4 s/c causing low voltage at (3).

VII/4   Set 3 is normal.
(1) Tr2, the UJT, is o/c, not discharging C1.
(2) C1 is s/c, or UJT s/c.
(4) Tr1 faulty, base-emitter s/c, collector o/c.
(5) D1 is s/c, shorting out the bias.
(6) R5 has gone high, hence low voltage at (1).

VII/5   Sets 4 and 5 are normal.
(1) Tr2 is faulty, base-emitter s/c, collector o/c.
(2) C2 is s/c (or collector-base s/c).
(3) VR1 value set too high.
(6) VR1 set too low, Tr1 is underbiased.
(7) C2 is o/c.

VII/6   Set 2 is normal.
(1) C3 is s/c.
(3) D1 is s/c.
(4) D6 high or C4 high.
(5) Tr1 is o/c.

VII/7   Set 4 is normal.
(1) Tr2 is faulty, base-emitter s/c, collector o/c.
(2) Tr4 is o/c or D1 o/c.
(3) Tr3 is o/c.
(5) D1 is s/c.
(6) R5 has gone high, restricting current in Tr4.

VII/8   Set 4 is normal.
(1) C1 is s/c.
(2) ZD1 is s/c.
(3) R3 has gone high.
(5) Tr1 has failed, high leakage between emitter and collector.
(6) IC1 faulty, not controlling.

SECTION VIII: DIGITAL & COUNTING CIRCUITS

VIII/1   Table 2 is normal.
(1) Flip-flop D is not working.
(3) o/c connection between D and A.
(4) Flip-flop B has failed.
(5) Flip-flop C has failed.
(6) Pin 2 or 3 is at high voltage.

VIII/2
(1) R3 is o/c.
(2) Connection between pin 11 of the SN7490 and pin 6 of the SN7447 is o/c.

(3) The connection to pin 8 of the SN7490 is earthed.
(4) Short between lines to pins 9 and 12 on the SN7490.
(5) Short between lines to pins 8 and 11 on SN7490.
(6) Short between pins or lines to pins 8 and 9 on SN7490.

VIII/3

(1) R4 high.
(2) R8 low.
(3) R1 low or R2 high.
(4) Leakage from pin 1 to pin 2 on IC1.
(5) o/c between pins 1 and 2 on IC1.
(6) Leakage between pins 3 and 4 on IC2.

VIII/4

(1) Gate IC4 is faulty, or gate IC7 faulty (more likely).
(2) Gate IC4 faulty.
(3) Faulty connection between pin 10 of IC1 and pin 1 of IC2.
(4) Clock pulse absent or o/c connection to clock terminals.

VIII/5

(1) Clock pulse absent or o/c connections.
(2) NOR gate faulty.
(3) NOR gate or inverter faulty.
(4) Link from pin 10 of IC1 to pin 1 of IC2 o/c.

VIII/6

(1) Preset voltage present on pins 4 or 8.
(2) Pin 16 earthed.
(3) Inverter faulty or o/c on pin 9 or 10.
(4) Decoding gates on D and E outputs faulty.

ELECTRONICS FAULT DIAGNOSIS

The object of this book is to provide an insight into typical circuits found in electronics equipment, with an emphasis on industrial and communications equipment, how they work and what can go wrong.

The pattern is to discuss the operation of each circuit, then to present a set of voltage readings or oscillograms which are to be interpreted by the reader. A complete set of diagnostic answers is provided in the last section of the book.

This book will be of considerable interest to the amateur wanting to learn about circuits and to test his understanding of them and will be of great value to the student since the book can be used progressively as an aid to the teaching of servicing, in particular to those taking the C & G 272 and 222 Courses and the future T.E.C. Courses.

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